REFERENCE MANUAL

Model 2108

VXI Serial Data System
Digital Resource Module

Manual Revision: 06/22/06
Manual Part Number: 2108RM001
Instrument Part Number:
30080/30150/30250

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(b) Ninety days for cables and adapters.

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PROTECT YOURSELF AND THE EQUIPMENT.
Follow these precautions:

- Don’t bypass the chassis’ power cord’s ground lead with two-wire extension cords or plug adapters.
- Don't disconnect the green and yellow safety-earth-ground wire that connects the ground lug of the chassis power receptacle to the chassis ground terminal.
- Don't energize the chassis until directed to by the installation instructions.
- Don't repair the instrument unless you are a qualified electronics technician and have instructions from Talon Instruments.
- Pay attention to the **WARNING** statements. They point out situations that can cause injury or death.
- Pay attention to the **CAUTION** statements. They point out situations that can cause equipment damage.
- Use ESD static control procedures when handling the 2108 or any of its modules.

Table of Contents

List of Figures

List of Tables

1 Introduction

The 2108 was designed to achieve two goals. First, to provide a test tool that can be easily programmed to emulate a wide range of serial buses in automated test applications. Second, to provide the design engineer with an interactive tool for development of a new serial bus, or modification of a standard serial bus.

The 2108 is preprogrammed with standard encoding and formatting schemes which allow the user to quickly emulate the most common serial buses. For modified or custom interfaces, programming is accomplished through an interactive software development package which can be mastered in a short time. For those with extremely complex tasks, the 2108 provides programming to the “bit” level using “micro code”.

Each transmit/receive module is coupled to the front panel via a UUT interconnect module. The interconnect modules are software configurable to support multiple signal types. Custom interconnect modules can be developed to meet the user’s requirements.

Figure 1-1 Talon 2108

1.1 Modular Design

The Model 2108 is a register based VXI module which provides for the fastest possible communication between the unit and the VXI controller. This allows data to be transferred in a continuous mode if required. The Model 2108 baseboard houses 1-4 serial channels and associated UUT interconnect modules. Each channel may be a transmitter or receiver and is addressed as an independent instrument. Adjacent transmitters and receivers may be operated as a bi-directional bus.

1.2 2108 Project Development Environment Software

The Model 2108 is shipped with VXI Plug&Play Win95,98 & NT compatible drivers. Included with the Model 2108 is an additional software package titled the 2108 Project Development Environment. This graphical software provides the user a means to program set-up instructions, download and upload data and interactively execute test routines. The test files generated may be saved for downloading and executing by the Plug&Play drivers using any standard Windows based test program.

A Serial Logic Analyzer application, which is used to view recorded data, provides a means for searching by trigger number or patterns. Users may define templates to aid in aligning and reading data streams. The software is excellent as a design tool for simulating new designs of custom or modified buses in the development lab.

1.3 2108TX Transmitter

The 2108TX Transmitter features data rates from 5 Kbps to 200 Mbps using internal or external clocks. It has software selectable data formats for the most used NRZ, Bi-phase or AMI formats. In addition users may program the 2108TX to inject errors, parity, or PRBS data. The two 4 Mbit memories may be used in a dual port mode to continually output data while reloading new data from the VXI controller.

1.4 Transmitter Interconnect Modules

The Transmitter Interconnect Modules provide the user with drivers to meet the electrical requirements of the UUT. Variable voltage drivers may be

programmed to meet a wide range of signal levels from ECL to +/- 15V in 20mV increments. In addition, drivers may be programmed as bi-polar, differential or trinary. Custom modules can be easily developed if off-the-shelf modules do not meet the user's requirements.

1.5 2108RX Receiver

The 2108RX Receiver records data at rates from 5 Kbps to 200 Mbps using internal or external clocks. It features clock recovery logic to sync to external clocks or data. Data capture may be initiated using 16 levels of 32 bit trigger patterns. The trigger compare logic provides signals that are routed to the adjacent channel that allows operations such as command/response or pre & post data capture based on the received data. The VXI controller may continually offload recorded data using the two 4 Mbit memories in a dual port mode.

1.6 Receiver Interconnect Modules

The Receiver Interconnect Modules provide for the physical connection to the UUT. The voltage detection range may be set as high as –15V to +15V with standard modules. Signal types may be programmed as bi-polar or differential. Software selectable impedance is provided and data rates to 200 Mbps are supported. Custom modules can be developed in those cases where standard modules do not meet the user's requirements.

2 Specifications

The following sections list the specifications of the 2108 Baseboard as well as the 2108TX and 2108RX.

2.1 General

VXI Bus Interface
- Register Based
- A16/D16/D32 Slave
- A24/A32 Required Memory[1] 4M/Channel
- Static/Dynamic Configuration[1]
- Output Low Sink Current (TTLTRG0 - TTLTRG7, IRQ1 - IRQ7) ..... 24 mA

Maximum number of serial channels 4
Dual Port Memory per channel 8Mbits
2108Tx
- Bit Rate ..... 5kbps to 200Mbps
- Pre-defined Bit Formats 12
  (NRZ-L/M/S, RTO, RTC, RTZ, Bi-Phase-L/M/S, DBi-Phase-M/S, AMI)
- Internal Clock Accuracy ..... 50 ppm
- Internal Clock Resolution ..... 4 digits
- Internal Clock Jitter ..... 30 ps rms, typ.
- Internal Clock Reference Source ..... Internal or External (20MHz)
- External Clock Frequency ..... 5KHz to 200MHz
- Sync Output ..... Yes (1)
  (TxSyncPulse)
- Data Markers ..... Yes (2)
  (TxMarker1 and TxMarker2)
- Output Flags ..... Yes (2)
  (TxFlagOut1 and TxFlagOut2)
- Input Flags ..... Yes (2)
  (TxFlagIn1 and TxFlagIn2)
- Error Injection ..... Yes
- Signal Delay ..... +/- 10ns
  (TxData, TxStrobe, TxClkOut, TxClkIn, TxMarker1, TxMarker2, TxSyncPulse)
- Signal Delay Resolution 1ns
  (TxData, TxStrobe, TxClkOut, TxClkIn, TxMarker1, TxMarker2, TxSyncPulse)
- Signal Offset ..... +/-3 Bits
  (TxMarker1, TxMarker2, TxBusy)
- Signal Offset Resolution ..... 1 Bit
  (NRZ-L, NRZ-M, NRZ-S, AMI)
- Signal Offset 2 Resolution ..... ½ Bit
  (RTO, RTC, RTZ, Bi-Phase-L, Bi-Phase-M, Bi-Phase-S, DBi-Phase-M, DBi-Phase-S)

2108Rx
- Bit Rate ..... 5kbps to 200Mbps
- Internal Clock Accuracy ..... 50 ppm
- Internal Clock Resolution ..... 4 digits
- Internal Clock Jitter ..... 30 ps rms, typ.
- Internal Clock Reference Source ..... Internal or External (20MHz)
- External Clock Frequency ..... 5KHz to 200MHz
- Clock Recovery ..... 5KHz to 200MHz
- Trigger Conditions 16
- Trigger Size ..... 64 bits max
- Trigger Sequence 16
- Trigger Qualifiers 2
  (RxQual1, RxQual2)
- Trigger Flags 5
  (RxTrigValid, RxTrigNum0, RxTrigNum1, RxTrigNum2, RxTrigNum3)
- Signal Timing Validation ..... Yes
  (RxG1Val, RxG0Val, RxClkOut)
- Signal Delay ..... +/- 10ns
  (RxData, RxClkIn)
- Signal Delay Resolution 1ns
  (RxData, RxClkIn)

Note 1: Switch Selection

2.2 Environmental

Temperature Range

Operating	0^{o} C to $+50^{o}$ C
Storage	-40^{o} C to $+70^{o}$ C (RH not controlled)

Altitude

Operating	Sea level to 10,000 ft.
Storage	Sea level to 40,000 ft.

Relative Humidity (non condensing)

0°C to +10°C	not controlled
+11°C to +30°C	95+/-5%RH
+31°C to +40°C	75+/-5%RH
+41°C to +50°C	45+/-5%RH

2.3 Size

Dimension

Single slot, “C” size VXI module. Approx. 26.22 cm x 3.04cm x 36.63 cm (10.325” x 1.2” x 14.42”)

Weight

< 1.81kg (4.0 lbs.)

2.4 Power Requirements

The power requirements are listed in table 2-1 below.

Voltage	Baseboard	2108TX	2108RX
	Peak (Amps)	Peak (Amps)	Peak (Amps)
+5V	1.5	.600	1.0
-5.2V	.100	0	0
-2V	0	0	0
+12V	0	0	0
-12V	.050	0	0
+24V	.050	0	0
-24V	.050	0	0

Table 2-1 Model 2108 VXI Power Requirements

2.5 Cooling Requirements

This section will guide the user through the necessary steps for calculating the total cooling requirements for any Model 2108 unit configuration.

The total power dissipated by the Model 2108 is equal to the sum of the individual power dissipations of its modular components. The modular components consist of the Baseboard Assembly, the Transmit/Receive Module(s) and the UUT Interconnect Module(s).

The first step is to document the Model 2108 configuration. Table 2-2 is the power dissipation worksheet. Transfer the module information from the Unit Configuration shipped with the 2108.

Position		Module Type	Power (W)
Baseboard		N/A	11.0
Channel 1	Module 1 (M1)		
	Module 2 (M2)		
Channel 2	Module 3 (M3)		
	Module 4 (M4)		
Channel 3	Module 5 (M5)		
	Module 6 (M6)		
Channel 4	Module 7 (M7)		
	Module 8 (M8)		
Total 2108 Power (W)			

Table 2-2 Model 2108 Power Dissipation Worksheet

After the Model 2108 unit configuration has been entered, locate and enter the appropriate power dissipation value in the space provided in Table 2-2 above.

Baseboard:

P = (+5V X 1.5A) + (|-5.2| X 100mA) + (|-12V| X 50mA) + (+24V X 50mA) + |-24V| X 50mA)

11.0W

2108TX:

P = (+5V X 600mA)

3W

2108RX:

P = (+5V X 1A)

5W

UUT Interconnect Modules:

Refer to the specific UUT Interconnect Module Reference Manual.

After entering the module power dissipation numbers add them together to determine the total 2108 power dissipation value (**P**).

The Model 2108 airflow requirement is calculated using the following equations:

Airflow (A) for 10°C rise (liters/sec):

A = P X 0.083

Airflow (A) for 20°C rise (liters/sec):

A = P X 0.0415

Where “P” is the total 2108 power dissipation from Table 2-2 above and “0.083” and “0.0415” are airflow in liters/sec per Watt (W).

3 Jumpers/Installation

The following sections describe the jumpers and hardware installation procedure for the 2108 baseboard, 2108Tx and 2108Rx modules. Refer to the appropriate appendix for the jumper description of specific interface modules.

3.1 2108 Baseboard Jumpers/Test Points/Switches

Figure 3-1 below shows the location of the jumpers, test points, switches and fuses on the 2108 baseboard PCB top side, part number 30081 revision 'C'. The PCB part number and revision can be located on the bottom of the PCB as shown in figure 3-2. Contact Talon Instruments for data on other versions of the 2108 baseboard.

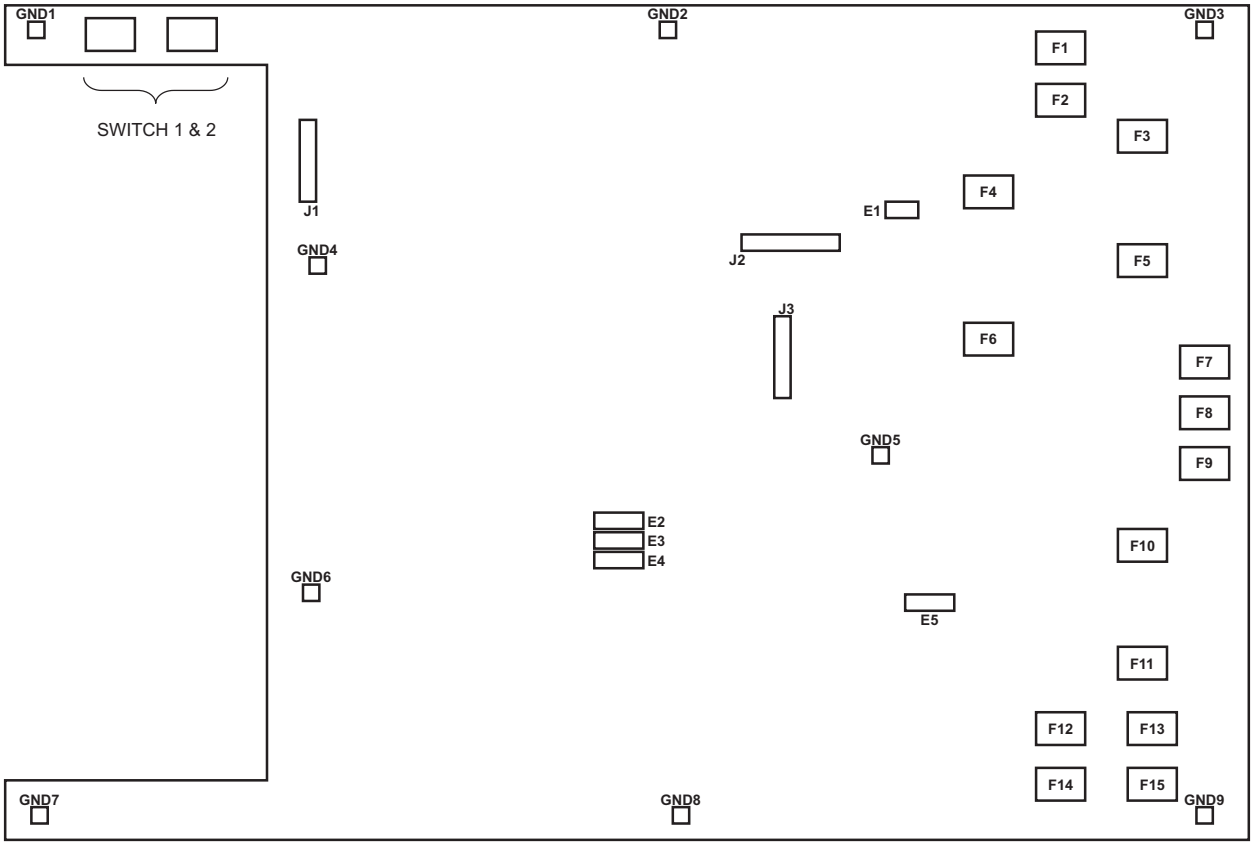


Figure 3-1 2108 Baseboard Top Side Jumper, Test Point, Switch and Fuse Locations

Figure 3-2 below shows the location of the jumpers, test points, switches and fuses on the 2108 baseboard PCB bottom side, part number 30081 revision ‘C’.

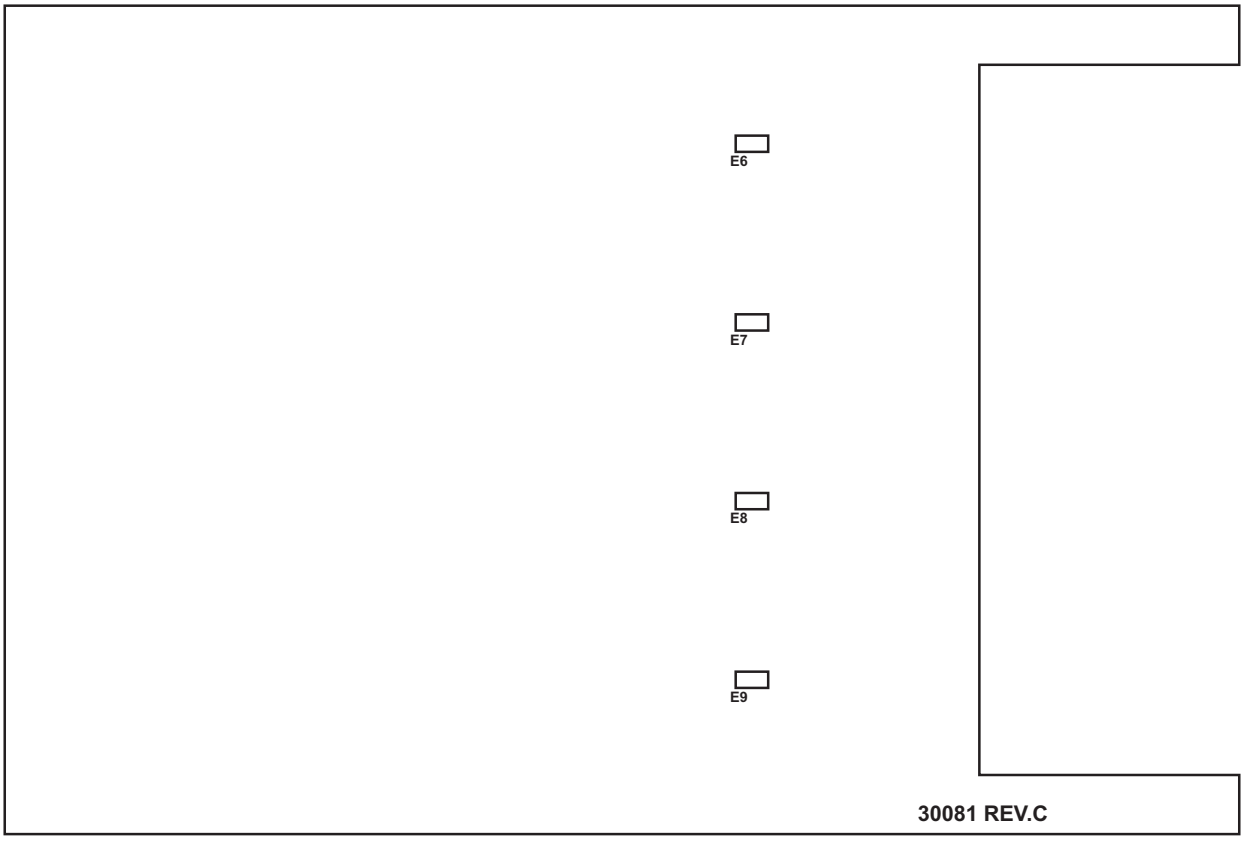


Figure 3-2 2108 Baseboard Bottom Side Jumper Locations

3.1.1 2108 Baseboard Test Point Description

Table 3-1 describes the test points on the 2108 Baseboard.

Mnemonic	Description
GND1	Probe Signal Ground.
GND2	Probe Signal Ground.
GND3	Probe Signal Ground.
GND4	Probe Signal Ground.
GND5	Probe Signal Ground.
GND6	Probe Signal Ground.
GND7	Probe Signal Ground.
GND8	Probe Signal Ground.
GND9	Probe Signal Ground.
J1	In-circuit Program Port for U13, U26, U38 and U60.
J2	In-circuit Program Port for U21.

Table 3-1 2108 Baseboard Test Point Description

3.1.2 2108 Baseboard Jumper Description

The following sections describe the 2108 Baseboard jumpers.

3.1.2.1 Serial PROM Data (E1)

This jumper is used to disconnect the serial PROM data output, U18 pin 40, from the FPGA for cable downloads.

Factory default: 0W resister shunt installed (serial PROM data connected to FPGA).

3.1.2.2 FPGA Mode (E2, E3, E4)

These jumpers set the FPGA mode pins.

Factory default: 0W resister shunt installed between E2 pins 2 and 3 (M0 low), E3 pins 2 and 3 (M1 low), E4 pins 1 and 2 (M2 high).

3.1.2.3 System Clock Select (E5)

This jumper selects the system clock source between the VXI backplane SYSCLK or 32MHz oscillator.

Factory default: 0W resister shunt installed between E5 pins 1 and 2 (32MHz selected)

3.1.2.4 Reference Logic Chain (E6, E7, E8, E9)

These jumpers are used to continue the reference logic in-circuit programming daisy chain.

Factory default: E6, E7, E8 and E9 shunts not installed.

3.1.3 2108 Baseboard Fuse Description

All of the fuses on the 2108 Baseboard are poly-fuses and will reset automatically.

Table 3-2 lists the voltage, usage and current rating for each fuse.

Fuse	Voltage	Usage	Max Current Rating 20° C
F1	-12V	-12V Bus	1.25A
F2	+12V	+12V Bus	1.25A
F3	+5V	+3.3V Channel 1 and 2 logic	2.6A
F4	+5V	+3.3V Baseboard logic	300mA
F5	+5V	+2.5 Channel 1 and 2 logic	2.6A
F6	+5V	+2.5V Baseboard logic+	300mA
F7	+5V	+5V Bus	2.6A
F8			2.6A
F9	-2V	-2V Bus	1.25A
F10	+5V	+3.3V Channel 3 and 4 logic	2.6A
F11	+5V	+2.5 Channel 3 and 4 logic	2.6A
F12	-5.2V	-5.2V Bus	2.6A
F13	-24V	-24V Bus	1.25A
F14	-5.2	-5.2V Bus	2.6A
F15	+24V	+24V Bus	1.25A

Table 3-2 2108 Baseboard Fuse Description

3.1.4 2108 Baseboard Switch Description

The following sections describes the 2108 Baseboard switch settings.

Figure 3-3 illustrates the 2108 Baseboard rev ‘C’ switches S1 and S2.

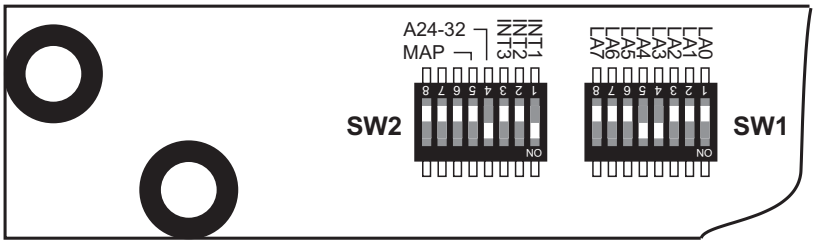


Figure 3-3 2108 Baseboard rev ‘C’ Switch Illustration

Figure 3-5 illustrates the 2108 Baseboard rev ‘B’ switches S1 and S2.

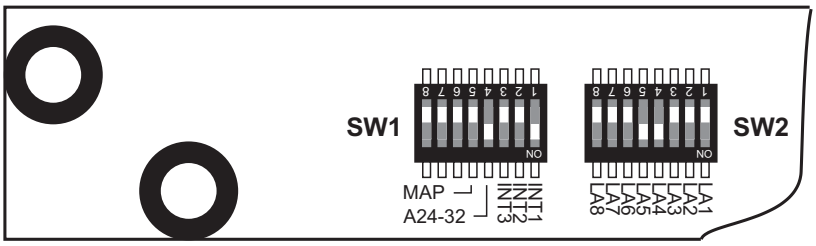


Figure 3-5 2108 Baseboard rev ‘B’ Switch Illustration

Figure 3-4 illustrates the 2108 Baseboard rev ‘NC’ switches S1 and S2.

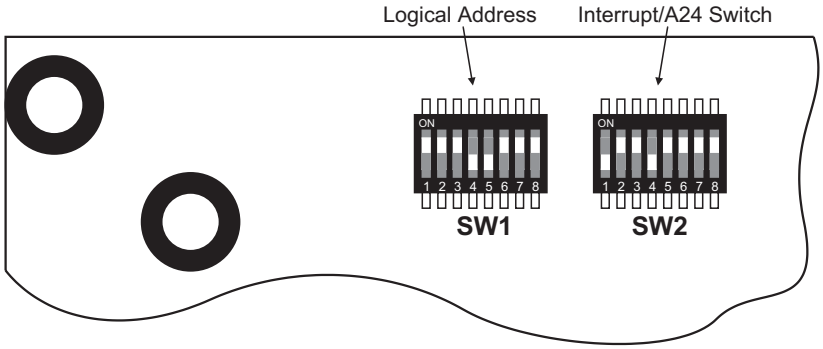


Figure 3-4 2108 Baseboard rev ‘NC’ Switch Illustration

The basebord revision is located on the back side etched in copper.

3.1.4.1 A32/A24, Interrupt, Map Switch

This switch is used to program the VXI interrupt level, A24/A32 selection as well as the A24/A32 map size.

The VXI interrupt level is programmed using the first three switchs positions. The interrupt level is decoded as shown in table 3-3 below.

Position 3	Position 2	Position 1	Interrupt Setting
UP	UP	UP	Disabled
UP	UP	DOWN	VXIRQ1
UP	DOWN	UP	VXIRQ2
UP	DOWN	DOWN	VXIRQ3
DOWN	UP	UP	VXIRQ4
DOWN	UP	DOWN	VXIRQ5
DOWN	DOWN	UP	VXIRQ6
DOWN	DOWN	DOWN	VXIRQ7

Table 3-3 2108 Baseboard Interrupt Switch Settings

The memory space each 2108 channel will request can be set to either A24 (position 4 up) or to A32 (position 4 down).

The size of the A24/A32 memory requested can be set to either 4M (position 5 up) or 2M (position 5 down).

The figures above shows an example where the interrupt setting is set to VXIRQ1 and the memory is set to A32 for 4M.

Factory Default: VXI interrupts disabled, A32 memory selected, 4M map size.

3.1.4.2 Logical Address Switch

This switch is used to program the logical addresses of the 2108 channels. Position 1 corresponds with the LSB of the logical address and position 8 corresponds with the MSB.

A logical address setting of 255 (all positions down, factory default) will enable the dynamic addressing mode. The logical address for each channel will be assigned by the resource manager. Logical address zero is reserved for the slot 0 controller and is invalid.

Any other logical address setting will cause the 2108 to request four consecutive logical addresses starting with the address coded on switch 2. The logical address setting must be a multiple of 4, the lower two logical address bits are ignored.

Channel one of each 2108 baseboard will be mapped to the lowest logical address assigned and channel four will be mapped to the highest.

The figures above shows an example where the logical address is set to 24 (position 5 and 4 down). This will cause the following logical address mapping:

Channel 1: LA24 (logical address 24)

Channel 2: LA25

Channel 3: LA26

Channel 4: LA27

3.2 2108 Transmitter Jumpers/Test Points

Figure 3-6 below shows the location of the jumpers and test points on the 2108 transmitter (2108Tx) PCB, part number 30151 revision 'N/C'.

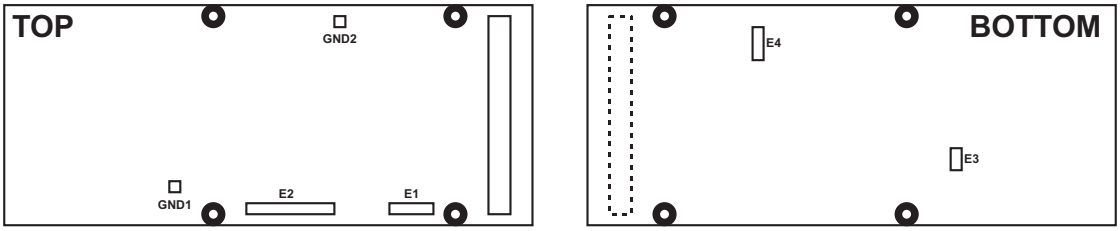


Figure 3-6 2108Tx Jumpers/Test Point Locations

3.2.1 2108Tx Test Point Description

Table 3-4 describes the test points on the 2108Tx.

Mnemonic	Description
GND1	Probe Signal Ground.
GND2	Probe Signal Ground.
E1	In-circuit Program Port for U4.
E2	In-circuit Program Port for U1 and U2.

Table 3-4 2108Tx Test Point Description

3.2.2 2108Tx Jumper Description

The following sections describe the 2108Tx jumpers.

3.2.2.1 Serial PROM Data (E3)

This jumper is used to disconnect the serial PROM data output, U4 pin 40, from the FPGA for cable downloads.

Factory default: 0W resister shunt installed (serial PROM data connected to FPGA).

3.2.2.2 FPGA Mode (E4)

This jumper sets the FPGA mode pins.

Factory default: 0W resister shunt installed between the center pad and the pad next to C59 (M0, M1, M2 low).

3.3 2108 Receiver Jumpers/Test Points

Figure 3-7 below shows the location of the jumpers and test points on the 2108 Receiver (2108Rx) PCB, part number 30251 revision 'N/C'.

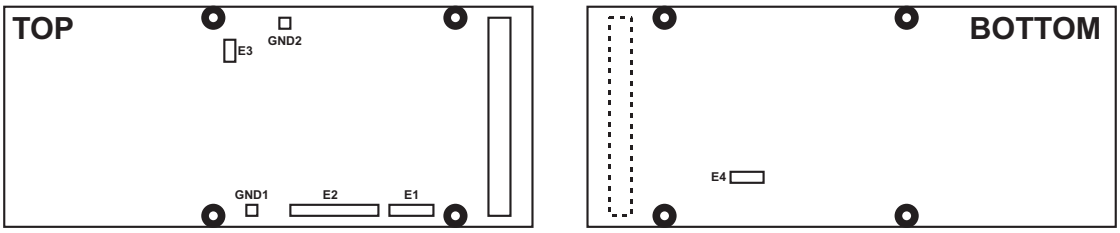


Figure 3-7 2108Rx Jumpers/Test Point Locations

3.3.1 2108Rx Test Point Description

Table 3-5 describes the test points on the 2108Rx.

Mnemonic	Description
GND1	Probe Signal Ground.
GND2	Probe Signal Ground.
E1	In-circuit Program Port for U15.
E2	In-circuit Program Port for U8.

Table 3-5 2108Rx Test Point Description

3.3.2 2108Rx Jumper Description

The following sections describe the 2108 Baseboard jumpers.

3.3.2.1 Serial PROM Data (E3)

This jumper is used to disconnect the serial PROM data output, U15 pin 40, from the FPGA for cable downloads.

Factory default: 0W resister shunt installed (serial PROM data connected to FPGA).

3.3.2.2 FPGA Mode (E4)

This jumper sets the FPGA mode pins.

Factory default: 0W resister shunt installed between the center pad and the pad next to C16 (M0, M1, M2 low).

3.4 Channel Module Installation

Each 2108 Baseboard can house up to four channels. Each 2108 channel includes either a 2108Tx or a 2108Rx module along with a corresponding UUT interface module.

Figure 3-8 below illustrates the channel positions of the 2108 and their module reference designators.

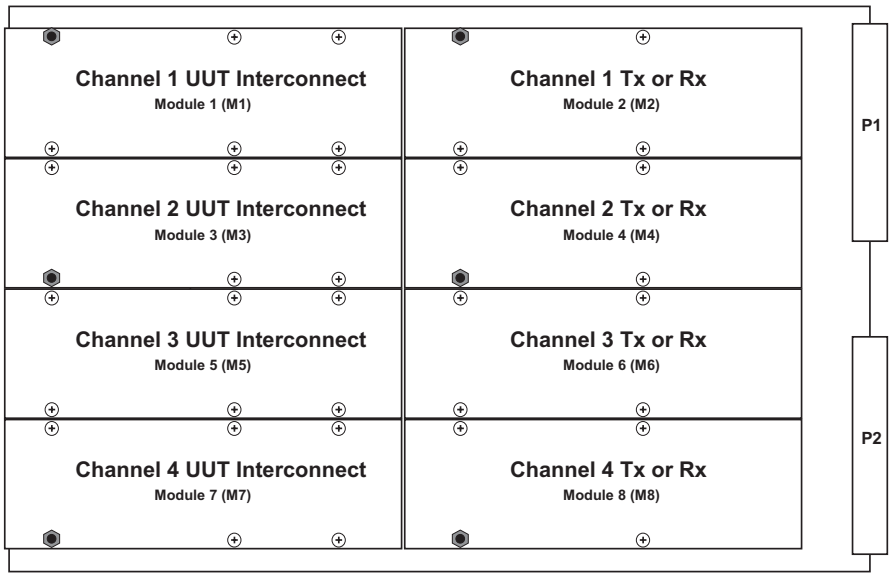


Figure 3-8 2108 Channel Module Positions

Perform the following steps to replace a 2108 channel:

Step 1. Using ESD protocols remove the 2108 from the VXI chassis.

Step 2. Remove the top cover screws.

Step 3. Remove the screws/spacers of the modules of the channel being replaced. Note the location of the spacers being removed for the top panel re-installation.

Step 4. Remove the Tx/Rx module first by grasping at each corner closest to the front panel and gently pulling up. Make sure to remove the module evenly to prevent damage to the high density P2 connector.

Step 5. Remove the UUT interface module by grasping at each corner furthest from the front panel and gently pulling up. Make sure to remove the module evenly to prevent damage to the high density P2 connector.

Step 6. Insert the new UUT interface module by lining up the connectors and gently pushing down evenly.

Step 7. Insert the new Tx/Rx module by lining up the connectors and gently pushing down evenly.

Step 7. Reinstall spacers and screws.

Step 8. Reinstall top cover.

4 Functional Description

The Talon 2108 is designed to be a general purpose serial bus emulator for use by design and test engineers. It contains many unique features to simplify serial data generation and recording. Unlike many testers, which test only a specific serial interface, the Talon 2108 provides a single instrument capable of testing a broad range of interfaces including custom or proprietary designs.

The 2108 consists of a baseboard and one or more transmit (Tx) or receive (Rx) channels. The following sections describe the 2108 baseboard as well as the transmitter and receiver modules. Refer to the specific UUT interconnect module reference manual for their functional descriptions.

4.1 2108 Baseboard (2108-BB)

The 2108-BB is used to route data and power from the VXI backplane to the channel slots. It also routes data between adjacent channel slots.

4.1.1 2108 Baseboard Block Diagram

Figure 4-1 below illustrate the 2108-BB block diagram.

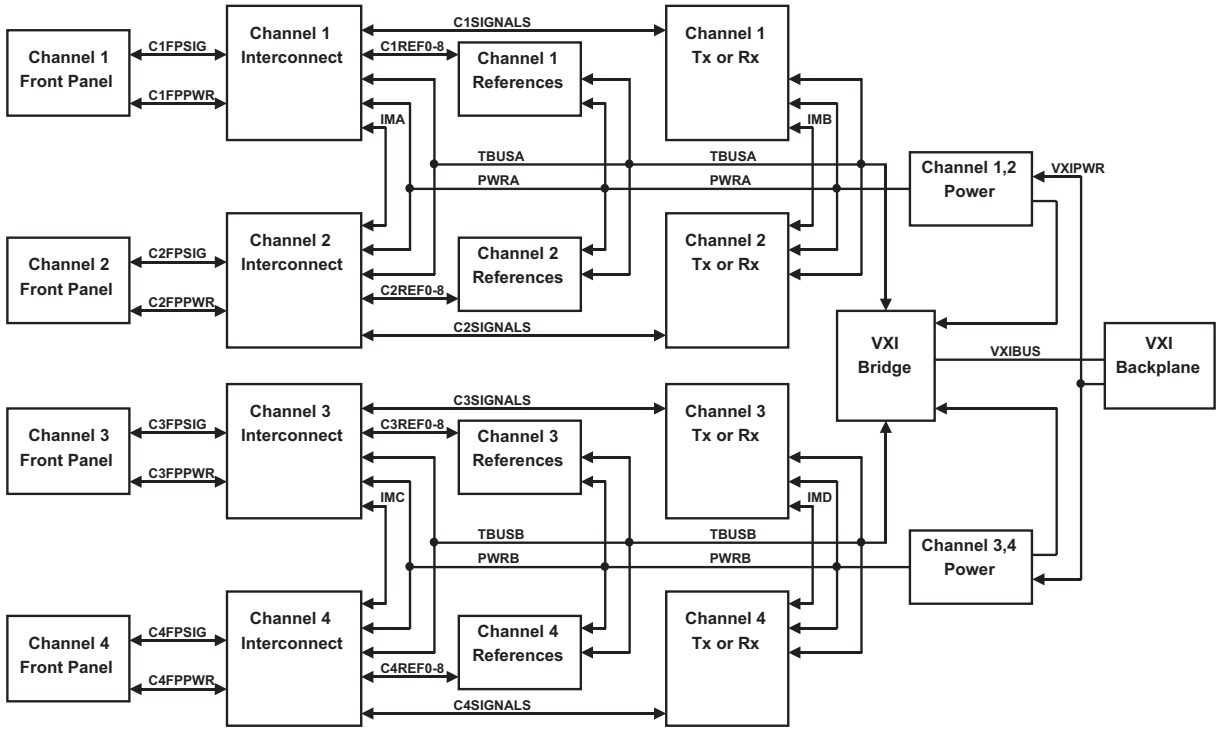


Figure 4-1 2108-BB Block Diagram

The following list describes the functional blocks shown in figure 4-1 above.

1. Channel 1-4 Front Panel — Physical connectors used to connect the 2108 channel to the users UUT/ITA.
2. Channel 1-4 Interconnect — Logic used to convert the 2108TX/2108RX signal level/format into UUT level/format.
3. Channel 1-4 References — Logic used to generate reference signals for the variable voltage interconnect modules.
4. Channel 1-4 Tx or Rx — Transmit/Receive logic and memory.
5. Channel 1,2 and 3,4 Power — Logic used to provide power to the baseboard and all its modules.
6. VXI Bridge — Logic used to translate VXIbus data transfers into 2108 transfers.
7. VXI Backplane — Physical connectors used to connect the 2108 to the VXIbus.

The following list describes the signals shown in figure 4-1 above.

1. CnFPSIG (n = 1 to 4) — I/O signals between the front panel and the interconnect module.
2. CnFPPWR (n = 1 to 4) — Front panel power inputs used by the variable voltage driver/receivers.
3. CnSIGNALS (n = 1 to 4) — Digital I/O signals between the 2108TX/2108RX and the interconnect module.

4.	CnREF0-8 (n = 1 to 4)	Reference signals used by the interconnect modules to specify VOH, VOL, VOZ, VIH, VIL and slew rate.
5.	TBUSA	I/O bus used to program channels one and two. The VXI bridge translates the VXIbus read/write cycles into TBUS read/write cycles.
6.	PWRA	Voltage bus used to provide power to channels one and two.
7.	IMA	Inter module bus that routes I/O signals between channels one and two interconnect modules.
8.	IMB	Intermodule bus that routes I/O signals between channels one and two 2108TX/2108RX modules.
9.	TBUSB	I/O bus used to program channel three and four. The VXI bridge translates the VXIbus read/write cycles into TBUS read/write cycles.
10.	PWRA	Voltage bus used to provide power to channels three and four.
11.	IMC	Intermodule bus that routes I/O signals between channels three and four interconnect modules.
12.	IMD	Intermodule bus that routes I/O signals between channels three and four 2108TX/2108RX modules.
13.	VXIPWR	VXIbus backplane power.
14.	VXIBUS	VXIbus I/O bus.

4.2 2108 Transmitter (2108TX)

The 2108TX is in a constant state of outputting data after power up. Figure 4-2 displays the operational state diagram of the 2108TX.

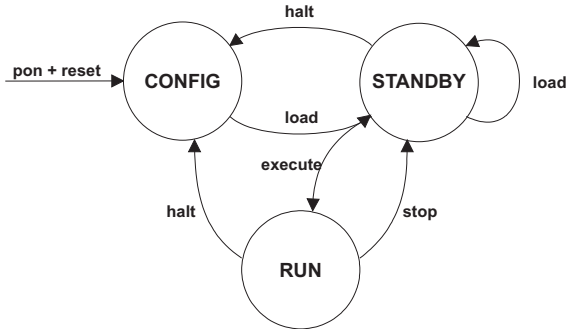


Figure 4-2 2108TX Operation State Diagram

CONFIG:
1. Drivers disabled.
2. CPU owns bank memory.

STANDBY:
1. Drivers enabled.
2. CPU owns bank memory.
3. Serial Processor outputs standby register.

RUN:
1. Drivers enabled.
2. Serial Processor owns bank memory.
3. Serial Processor outputs specified CMT with Idle during dead time.

The functional architecture of the 2108TX is shown in figure 4-3.

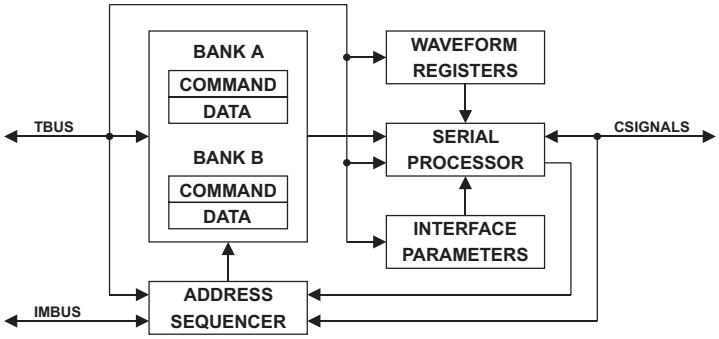


Figure 4-3 2108TX Block Diagram

The following list describes the functional blocks shown in figure 4-3 above.

1.	Bank Memory	Defines the output data and how to process it.
2.	Waveform Registers	Defines output data that bypasses the serial processor.

3. Serial Processor — Takes the data from the bank memory and applies the associated command for output.
4. Interface Parameters — Specifies the clock source, bit rate, bit encoding, signal routing and UUT interconnect settings.
5. Address Sequencer — Programs the order in which the bank memory is sent to the serial processor.

The following list describes the signals shown in figure 4-3 above.

1. TBUSA — I/O bus used to program the 2108TX. The VXI bridge translates the VXIbus read/write cycles into TBUS read/write cycles.
2. CSIGNALS — Digital I/O signals to/from the 2108TX.
3. IMBUS — Intermodule bus that routes I/O signals between channels.

4.2.1 2108TX Bank Memory

The bank memory defines the desired data and how to process that data. The user segments the bank memory into “Control Memory Tables” which consists of a *Name* and a *size*, from 1 to 512K words. Each word contains 8 bits for data and 8 bits for command. The command field controls the “Serial Processor” and defines the source and number of bits to output. Figure 4-1 gives the internal format of a Bank Memory Table word.

Command								**Data**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M1	M2	TYPE			INDEX			DINDEX							

Table 4-1 2108TX Bank Memory Format

4.2.1.1 Marker Bits (“M1 and M2")

Marker bits, M1 and M2, are auxiliary signals, which are output on the 2108 and can be programmed to accompany the data or waveform transmissions. They come out the front panel 36 pin connector and may be used for “data valid” signals or other synchronous signals. They may be programmed to either a high or low state (0 = low, 1 = high) and are held in that state for the entire word.

At the hardware level, the engineer must fill the Bank Memories (A & B) with appropriate commands and data to emulate a particular interface. The Bank Memories may be subdivided into tables referred to as Control Memory Tables or CMT’s. A Control Memory Table may be of any length up to the limit of the memory depth. As defined later, a Control Memory Table defines the unique serial data and how to transmit that data. The two memories may be used in a ping-pong manner to facilitate continuous data output.

4.2.1.2 Output Type (“TYPE”)

The nature of serial transmissions is repetitive patterns with varying data content. The pattern may be data only with sync codes, a special sync waveform followed by data, a dead time or gap time preceding either of the patterns above, etc. In order to support these various patterns, the 2108 provides “TYPE commands” to allow the user to define the structure or segments of his serial pattern.

Bit 13	Bit 12	Bit 11	Output Type
0	0	0	Waveform.
0	0	1	Reserved.
0	1	0	Programmable Gap.
0	1	1	Transmitter Gap (Fixed/Random).
1	0	0	LUT data.
1	0	1	LUT data with parity.
1	1	0	PRBS.
1	1	1	PRBS with parity.

The TYPE commands available to define the segment types of the serial pattern are:

Waveform — Special Waveform. This TYPE command ignores the contents of the “DATA” field and transmits the contents of the Waveform Parameter Register defined by the “INDEX” field. Some protocols use invalid waveforms for sync or special data encoding patterns.

Programmable Gap — Pause Waveform (for a number of bit times). This TYPE command uses the contents of the DATA field to generate a pause waveform for the number of bit times (4 -255) as specified in the DATA field. The user selects the waveform to output

during the gap using the “INDEX” field. This is useful if neither a fixed nor purely random intermessage gap is desired. Using this command, one can vary the gap time under controlled conditions.

Transmitter Gap Intermessage Gap for fixed or random time. Some protocols like 1553 and ARINC 429 require a minimum intermessage gap, but not a maximum. This TYPE command allows the insertion of a GAP of either a fixed or random time between upper and lower limits. The user selects the waveform to output during the gap using the “INDEX” field. The upper and lower limits are specified in the RUN Parameters entries.

LUT Data Data only. This TYPE command will output the contents of the lookup table (LUT) specified by the “INDEX” field and indexed by the “DINDEX” field. Parity is accumulated but not appended.

LUT Data with Parity Data with parity appended. This TYPE command will output the contents of the lookup table (LUT) specified by the “INDEX” field and indexed by the “DINDEX” field with a parity bit appended. If preceding fields were DATA types the accumulated parity is appended. Parity type (odd or even) is specified under RUN parameters.

PRBS This type is similar to the “DATA” type but instead of the contents of the LUT data field a Pseudo Random Bit Sequence is output. Parity is accumulated but not output.

PRBS with Parity This type is similar to the “DATA” type but instead of the contents of the LUT data field a Pseudo Random Bit Sequence is output. The accumulated parity is appended.

4.2.1.3 “INDEX” Field

The “INDEX” field points to either the Waveform Parameter Register (WPR0 – WPR7) or the LUT depending on the “TYPE” field.

4.2.1.4 “DINDEX” Field

The “DINDEX” field specifies the LUT index or the programmable gap size depending on the “TYPE” field.

4.2.2 2108TX Waveform Registers

The waveform registers allow the user to specify the number of bits in each of the eight waveforms as well as the reference group to use if a variable voltage UUT interconnect module is installed.

4.2.3 2108TX Serial Processor

The serial processor is comprised of eight LUT Memories, sixteen Data Format Registers and sixteen Bit Format Codes.

4.2.4 2108TX Interface Parameters

The Interface Parameters specify how the “Serial Processor” outputs data, i.e., the clock source, bit encoding, signal routing, signal delay, signal offset and UUT interconnect settings (termination, reference levels, driver configuration).

4.2.5 2108TX Address Sequencer

The Address Sequencer controls the order in which the “Serial Processor” receives data from the bank

memory. The address sequencer is programmed using a 1024 deep instruction memory. Table 4-2 lists the 2108 Address Sequencer instructions.

COMMAND	SUBCODE	PARAMETERS	FUNCTIONAL DECRIPTION
SET WORD COUNT	IDLE	WORD COUNT,(1-512K)	Sets the IDLE CMT (Command Memory Table) word count register
	CMT	WORD COUNT,(1-512K)	Sets the TRANSMIT CMT (Command Memory Table) word count register
TRANSMIT	IDLE	BANK ADDRESS (0-3FFFFh) BANK SELECT, (A or B) PARITY,(Odd,Even,Hold,Resume) RESEED PRBS, (Yes or No)	Output data from specified bank memory for IDLE WORD COUNT words when not busy.
	IDLE ONE WORD		Output data from specified bank memory for one word when not busy.
	CMT	BANK SELECT, (A or B) PARITY,(Odd,Even,Hold,Resume) RESEED PRBS, (Yes or No)	Set busy and output data from specified bank memory for CMT WORD COUNT words.
	CMT ONE WORD		Set busy and output data from specified bank memory for one word.
	RESUME	BANK SELECT, (A or B) PARITY,(Odd,Even,Hold,Resume) RESEED PRBS, (Yes or No)	Set busy and output data from last memory plus one for CMT WORD COUNT words.
	RESUME ONE WORD		Set busy and output data from last memory plus one for one word.
DEFINE	LOOP COUNTER 0	COUNT, (1-64K)	Set the loop counter to specified value.
	LOOP COUNTER 1		
	LOOP COUNTER 2		
	LOOP COUNTER 3		
	FP FLAGS	ENABLE, (Yes or No) LEVEL, (High or Low) MASK, (Change or No change)	Simultaneous programming of Front Panel Output Flags 1 and 2. MASK allows programming of either flag without altering contents of the other flag register.
	GP FLAGS	ENABLE, (Yes or No) LEVEL, (High or Low) MASK, (Change or No change)	Simultaneous programming of General Purpose Output Flags 1 and 2. MASK allows programming of either flag without altering contents of the other flag register.
	RECEIVER FLAGS	CMDNUM[3:0] MODE, (Single or Multi mode	Set Mode and CMDNUM bits 3 to 0 to Rx Module via the 2108 Inter-module bus. Causes RxStatrcmd strobe to be generated.
SET CONTROLS	REQUEST BANK A	NONE	Address Sequence request for Bank A memory.
	REQUEST BANK B	NONE	Address Sequence request for Bank B memory.
	RELEASE BANK A	NONE	Address Sequence release Bank A memory.
	RELEASE BANK B	NONE	Address Sequence release Bank B memory.
	HALT CMT	NONE	Stops the current CMT output and returns to IDLE.
REPEAT	NONE	COUNT, (1-64K)	Repeat the next command for the specified count, must be a non-jump command.
NOP	NONE	NONE	No-op.
JUMP	UNCONDITIONAL	JUMP ADDRESS, (0-1023) SUBROUTINE FLAG, (True or False)	Jump to the specified address. If the subroutine flag is set, save the next address as the return address.
	LOOP COUNTER	JUMP ADDRESS, (0-1023) ZERO, (True or False) SUBROUTINE FLAG, (True or False)	Jump to the specified address if the loop counter is zero/not zero. If the subroutine flag is set, save the next address as the return address.
	FP FLAGS	JUMP ADDRESS, (0-1023) STATE, (High, Low, Rising or Falling) SUBROUTINE FLAG, (True or False)	Jump to the specified address if the front panel flag matches the specified state. If the subroutine flag is set, save the next address as the return address.
	GP FLAGS	JUMP ADDRESS, (0-1023) JAR FLAG, (True or False) STATE, (High, Low, Rising or Falling) SUBROUTINE FLAG, (True or False)	Jump to the specified address if the general purpose flag matches the specified state. If the subroutine flag is set, save the next address as the return address.
	RECEIVER FLAG	JUMP ADDRESS, (0-1023) VECTORED, (True or False) STATE, (True or False) SUBROUTINE FLAG, (True or False)	Jump to the specified address (vectored or non vectored) if the receiver flag (RxTrigValid) is true or false. Generate a TxAck if enabled. If the subroutine flag is set, save the next address as the return address.
	BUSY FLAGS	JUMP ADDRESS, (0-1023) MODULE, (Tx or Rx) STATE, (Busy or Not busy) SUBROUTINE FLAG, (True or False)	Jump to the specified address if the busy flag is true or false. f the subroutine flag is set, save the next address as the return address.
	BANK GRANT	JUMP ADDRESS, (0-1023) STATUS, (Granted or Not granted) SUBROUTINE FLAG, (True or False)	Jump to the specified address if the bank grant flag is true or false. f the subroutine flag is set, save the next address as the return address.
	BANK FULL	JUMP ADDRESS, (0-1023) STATUS, (Full or Not Full) SUBROUTINE FLAG, (True or False)	Jump to the specified address if the bank full flag is true or false. f the subroutine flag is set, save the next address as the return address.
	BREAKPOINT	NONE	Halts command execution until user resumes
	RETURN	NONE	Return from a subroutine jump.

Table 4-2 Address Sequence Command Listing

4.3 2108 Receiver (2108RX)

The 2108RX can be programmed to record up to sixteen trigger sequences. The user can specify the trigger pattern(s), qualifier state, pre-trigger record depth, post trigger record depth and loop count for each trigger sequence.

Figure 4-4 shows the operation state diagram of the 2108RX.

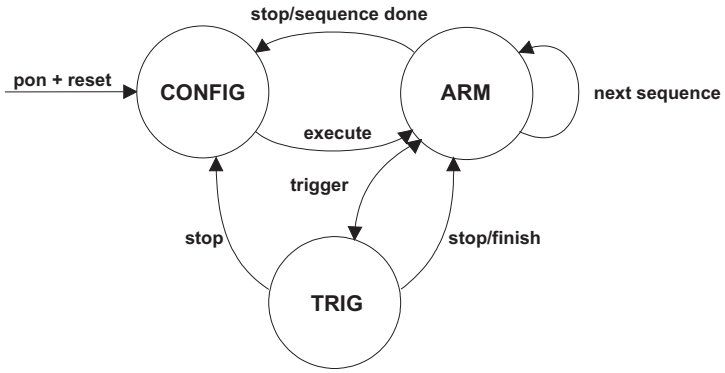


Figure 4-4 2108RX Operation State Diagram

CONFIG:
1. Load trigger/qualifier memory.
2. Clear input pipeline.
3. Pre-load record memory.

ARM:
1. Trigger logic enabled.
2. Pre-trigger data recording.

TRIG:
1. Trigger valid generated.
2. Post-trigger data recording.

The functional architecture of the 2108TX is shown in figure 4-5.

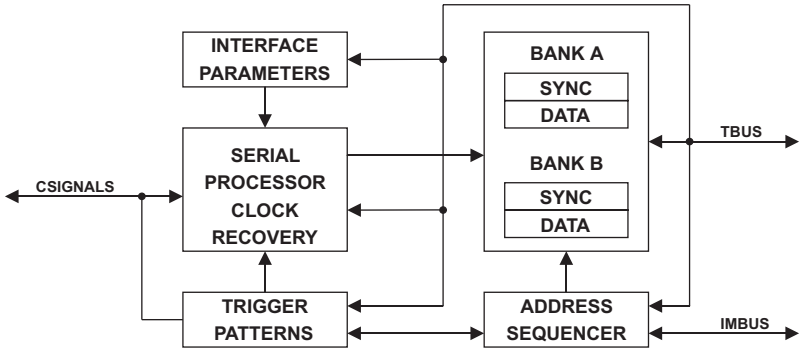


Figure 4-5 2108RX Block Diagram

The following list describes the functional blocks shown in figure 4-5 above.

1.	Interface Parameters	Specifies the clock source, bit rate, bit encoding, signal routing and UUT interconnect settings.
2.	Bank Memory	Stores the input data and how it was recorded.
3.	Serial Processor	Takes the serial data from the UUT interconnect, compares it against the trigger patterns and stores it in the bank memory along with sync data.
4.	Clock Recovery	Logic to recover a clock from the input data.
5.	Trigger Patterns	Memory to define the trigger patterns.
6.	Address Sequencer	Programs the trigger enable, qualifier state and pre/post trigger record depth.

The following list describes the signals shown in figure 4-5 above.

1.	CSIGNALS	Digital I/O signals to/from the 2108RX.
2.	TBUSA	I/O bus used to program the 2108RX. The VXI bridge translates the VXIbus read/write cycles into TBUS read/write cycles.
3.	IMBUS	Intermodule bus that routes I/O signals between channels.

4.3.1 2108RX Interface Parameters

The Interface Parameters specifies how the “Serial Processor” inputs data, i.e., the clock source, bit encoding, signal routing, signal delay, signal offset and UUT interconnect settings (termination, reference levels, receiver configuration).

4.3.2 2108RX Bank Memory

The bank memory stores the data from the receiver board as well as sync and time stamp data.

Table 4-3 lists the bit format of the receiver bank memory.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X								SYNC								GOOD1								GOOD0							

Table 4-3 2108RX Bank Memory Format

4.3.2.1 Recorded Data (”GOOD1” and “GOOD0”)

Data is loaded into the GOOD0 and GOOD1 memory from MSB to LSB, i.e., MSB is oldest data bit. A ‘one’ indicates a valid level. Figure 4-6 illustrates the GOOD1/GOOD0 decoding.

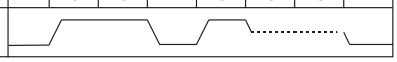
GOOD 0 = 68h	0	1	1	0	1	0	0	0
GOOD 0 = 91h	1	0	0	1	0	0	0	1
WAVEFORM								

Figure 4-6 Record Data Decoding

4.3.2.2 Record Data Sync (”SYNC”)

The SYNC byte provides information to the user that is used to reconstruct the record memory. The following table describes the data fields of the sync byte.

Bit #							
23	22	21	20	19	18	17	16
TYPE DATA					TYPE		

The fields of the sync byte contains data dependant on the sync type (”TYPE”). The following table describes the sync types as well as the sync type data.

Bit #							
23	22	21	20	19	18	17	16
NU					PRE (0)		
TNUM				NU	TRIG (3)		
TSDATA				NU	TS (5)		
NU					POST (6)		
STEP				FULL	TBIT (7)		

PRE	Preamble or invalid data (invalid data is GOOD0 = GOOD1 = 1, all other combinations of GOOD0 and GOOD1 is pre trigger)
TRIG	Trigger Type (data is post trigger)
TNUM	Trigger number that initiated record sequence.
TS	Time Stamp Type (data is post trigger)
TSDATA	Time stamp nibble (LSN to MSN)
POST	Postamble data
TBIT	Trigger bit flag (data from previous address contains LSB of trigger, data at this address is post trigger)
FULL	Allocated preamble memory full (1 = full)

STEP Sequence step that initiated the record sequence

Notes:

1. The sync byte at the address prior to the “TBIT” will contain a “1” that indicates the LSB position of the trigger.
2. It takes eight TS types to capture the entire 32 bits of time stamp data.

Example 1:

Preamble count = 8

Postamble count = 10

Address	Sync	Description
0	0x00	Preamble
4	0x00	Preamble
8	0x00	Preamble
12	0x20	Bits 7, 6 preamble, Bit 5 trigger LSB, Bits 4-0 postamble
16	0x07	Sync, Step = 0, FULL = 0
20	0x00	Invalid
24	0x00	Invalid
28	0x00	Invalid
32	0x23	Postamble, trigger = 2
36	0x15	Postamble, time stamp 3-0 = 1
40	0x25	Postamble, time stamp 7-4 = 2
44	0x35	Postamble, time stamp 11-8 = 3
48	0x45	Postamble, time stamp 15-12 = 4
52	0x55	Postamble, time stamp 19-16 = 5
56	0x65	Postamble, time stamp 23-20 = 6
60	0x75	Postamble, time stamp 27-24 = 7
64	0x85	Postamble, time stamp 31-28 = 8
68	0x06	Postamble
72	0x00	Next Preamble

Reconstructed stream address:

0,4,8,12,16,32,34,36,40,44,48,52,56,60,64,68

Trigger LSB at address 12 bit 5

Step = 0

Trigger = 2

Time stamp = 0x87654321

Example 2:

Preamble count = 10

Postamble count = 12

Address	Sync	Description
0	0x00	Preamble
4	0x00	Preamble
8	0x00	Preamble
12	0x01	Bits 7-1 preamble, Bit 0 trigger LSB
16	0x3F	Sync, Step = 3, FULL = 1
20	0x00	Preamble
24	0x00	Preamble
28	0x00	Preamble
32	0x00	Preamble
36	0x00	Preamble
40	0x73	Postamble, trigger = 7

44	0xF5	Postamble, time stamp 3-0 = F
48	0xE5	Postamble, time stamp 7-4 = E
52	0xD5	Postamble, time stamp 11-8 = D
56	0xC5	Postamble, time stamp 15-12 = C
60	0xB5	Postamble, time stamp 19-16 = B
64	0xA5	Postamble, time stamp 23-20 = A
68	0x95	Postamble, time stamp 27-24 = 9
72	0x05	Postamble, time stamp 31-28 = 0
76	0x06	Postamble
80	0x06	Postamble
84	0x06	Postamble
88	0x00	Next Preamble

Reconstructed stream address:

20,24,28,32,36,0,4,8,12,16,40,44,48,52,56,60,64,68,72,76,80,84

Trigger LSB at address 12 bit 0

Time stamp = 0x9ABCDEF

Step = 3

Trigger = 7

Example 3:

Preamble count = 4

Postamble count = 5

Address	Sync	Description
0	0xEF	Sync, Step = 15, FULL = 1
4	0x00	Preamble
8	0x00	Preamble
12	0x80	Bits 7 trigger LSB, Bits 6-0 postamble
16	0x03	Postamble, trigger = 0
20	0x85	Postamble, time stamp 3-0 = 8
24	0x65	Postamble, time stamp 7-4 = 6
28	0x45	Postamble, time stamp 11-8 = 4
32	0x25	Postamble, time stamp 15-12 = 2
36	0x00	Next Preamble

Reconstructed stream address:

4,8,12,0,16,20,24,28,32

Trigger LSB at address 12 bit 7

Step = 15

Trigger = 0

Time stamp = 0xXXXX2468

4.3.3 2108RX Serial Processor

The serial processor receives data from the UUT interconnect module and stores it along with sync information into the bank memory. While the data is being recorded, it is compared to the trigger patterns. When a pattern match if found a trigger valid signal is generated.

4.3.4 2108RX Clock Recovery

The clock recovery logic is comprised of a High Frequency Clock Recovery (HFCR) and a Low Frequency Clock Recovery (LFCR) circuit. The user can select the recovered clock, generated from the input data, as the input data strobe.

4.3.5 2108RX Trigger Patterns

The trigger pattern logic contains sixteen 32 bit registers. Each trigger pattern register can be programmed to detect valid high, valid low, don't care and invalid data bit patterns. The sixteen 32 bit registers can also be configured as eight 64 bit registers for longer pattern requirements.

4.3.6 2108TX Address Sequencer

The address sequencer is comprised of sixteen record registers. Each record register specifies a trigger mask, qualifier mask, pre-trigger size, post trigger size, handshake flag and last sequence flag.

Appendix A Glossary

Bipolar	One signal represents a state.
Comparator	Compares an input signal with a reference level
Differential	A pair of signals which represent a state. Also, when one is at a high level the other is at a low level and vice-versa.
Driver fault	The output driver (for S1 thru S8) is shut down due to current overloading or over temperature
ECL	Emitter coupled logic
FlagIn	An input signal which the transmitter can query
FlagOut	An output signal which the transmitter can query
Good “0”	A signal generated when an input signal is less than VIL
Good “1”	A signal generated when an input signal is greater than VIH
HFCR	High Frequency Clock Recovery
LED	Light Emitting Diode
LFCR	Low Frequency Clock Recovery
Marker	An output signal used to mark one or more portions of the output data stream
Reference	A programmable DC voltage
RX01	Model 1 Receiver Interconnect Module
RxArm	Record sequence “ARMed” and waiting for a trigger
RxBusy	Record sequence running
RxCLKOUT	An output signal of “Clock In” used to align data wrt clock
RxG0Val	An output signal of “Good-0” used to align data wrt clock
RxG1Val	An output signal of “Good-1” used to align data wrt clock
RxTrigNumber	The particular trigger number which occurred for a particular trigger event
RxTrigValid	Trigger valid signal generated by the receiver when a trigger has occurred
RxWait	Receiver is waiting for an acknowledge of a Trig Valid
Slew rate	Rate of change of an output transition (typ in V/ns)
SMA	A small screw-on RF connector
SyncPulse	An output pulse which can be positioned in relation to the output data stream (typically used to synchronize another instrument).
TrigDis	Trigger disabled in the receiver (in post trigger or waiting for a TxAck)
Trinary	Three distinct levels
Tri-state	A third state indirectly occurring when not being driven to a defined state.
TX01	Model 1 Transmitter Interconnect Module
TxAck	A signal from the transmitter sent to the receiver acknowledging that a trigger has been captured
TxBusy	Transmitter running
TxCLKOUT	A time adjustable (also inventable) representation of the clock used by the transmitter
UUT	Unit Under Test
V+	Positive supply voltage provided by the user
V-	Negative supply voltage provided by the user
VOH	A reference defining an Output High Level

VOL	A reference defining an Output Low Level
VOZ	A reference defining an Output third state level.
VIH	A reference defining an Input High Level
VIL	A reference defining an Input Low Level
VXI	VME Extensions for Instrumentation

Appendix B 2108 Register Map

The Talon 2108 addressing is split into two sections, A16 and A24/A32. The two sections are selected by six signals on the VXI backplane called the address modifiers.

The 2108 will respond to the following A16 address modifier settings: hex 29 and 2D.

If the 2108 is set to A24 addressing (section) then it will respond to the following address modifier settings: hex 39, 3A, 3B, 3D, 3E and 3F.

If the 2108 is set to A32 addressing (section) then it will respond to the following address modifier settings: hex 39, 3A, 3B, 3D, 3E and 3F.

1 2108 Baseboard A16 Map

Every VXI device is identified by a unique number called the logical address (LA). The base address of the A16 memory is calculated from the LA using the following formula:

$A16_{base} = (LA \times 40_h) + C000_h$

For Example:

LA = 4

A16base $= (4 \times 40_h) + C000_h$

$= C100_h$

The first four A16 registers and their function are defined by the VXI standard. The remaining A16 registers are 2108 specific.

Register	Offset	R/W	Description
ID/LA	0h	read	Instrument ID Register
		write	Logical Address Register
DEVICE	2h	read	Device Register
STATUS/CONTROL	4h	read	Status Register
		write	Control Register
OFFSET	6h	read/write	A32/A24 Offset Register
REV	20h	read	Baseboard Revision Register
ID	22h	read	Baseboard ID Register
TRIG	24h	read/write	Trigger Routing Register
COND	26h	read	Condition Register
PTE	28h	read/write	Positive Transition Event Enable Register
NTE	2Ah	read/write	Negative Transition Event Enable Register
EVENT	2Ch	read	Event Register
ENABLE	2Eh	read/write	Interrupt Enable Register
INTR	30h	read	Interrupt Level Register
PWR/TEMP	32h	read	Power/Temperature Monitor Register
PAGE	34h	read/write	A24 Memory Page Register

Table B-1 A16 Address Map

The following sections describes the registers listed above.

1.1 ID Register

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Device Class		Address Space		Manufacturer ID											

Field/Bit Description:

Device Class	Specifies the VXI device classification: 2108 = hex 3 (register based).
Address Space	Device address mode; 2108 = hex 1 (A16/A32) or hex 0 (A16/A24) based on the CPU switch setting, see section
Manufacturer ID	Unique ID; Talon Instruments = hex F0F.

1.2 LA Register

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Logical Address															

Field/Bit Description:

Logical Address — Specifies the logical address if dynamic configuration is enabled, see section

1.3 Device Register

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Required Memory				Device Type											

Field/Bit Description:

Required Memory — Specifies the amount of A24/A32 memory addressing required; 2108Tx = 4M, 2108Rx = 4M, Empty Slot = 0.

Device Type — Unique device identifier; 2108Tx = hex 110, 2108Rx = hex 120, Empty slot = hex 130.

1.4 Status Register

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A24/A32 Active	MODID	NU										Ready	Passed	NU	

Field/Bit Description:

A24/A32 Active — Indicates whether the A24/A32 memory space is enabled (1) or disabled (0).

MODID — A zero in this field indicates that the 2108 is selected by a high state on the P2 MODID line.

Ready — A zero in this field indicates that the 2108 is still in the self test/initialize state during power up. A one in this field with a zero in the “passed” field indicates the 2108 failed register initialization. A one in this field along with a one in the “passed“ field indicates the 2108 is operational.

Passed — A zero in this field indicates the 2108 is either executing or has failed self test. A one indicates the 2108 has passed self test and is ready for operation.

1.5 Control Register

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A24/A32 Enable	NU													Sysfail Inhibit	Reset

Field/Bit Description:

A24/A32 Enable — A one (1) enables access to the A24/A32 registers of the 2108. A zero (0) disables access.

Sysfail Inhibit — A one (1) in this field disables the 2108 from driving the SYSFAIL line.

Reset — A one (1) in this field forces the 2108 into the reset state.

1.6 Offset Register

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A24 MSA	NU														
A32 MSA										NU					

Field/Bit Description:

A24 MSA — This bit is mapped to the most significant bit of the A24 address decoder.

A32 MSA — These 9 bits are mapped to the upper 9 bits of the A32 address decoder.

1.7 REV Register

This register contains the revision and version of the 2108 Baseboard.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Version								Revision							

Field/Bit Description:

Revision — These bits indicate the revision of the 2108 Baseboard.
Version — These bits indicate the version of the 2108 Baseboard.

1.8 ID Register

This register contains the identification code of the 2108 Baseboard.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID															

Field/Bit Description:

ID — These bits indicate the id code of the 2108 Baseboard.

1.9 TRIG Register

Each 2108 channel has an output trigger (TRIGB) and an input trigger (TRIGA). This register programs the input trigger source as well as the output trigger routing.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU								TRIGB				TRIGA			

Field/Bit Description:

TRIGA — These bits select the TRIGA source according to the table below:

Bit 3	Bit 2	Bit 1	Bit 0	TRIGA Source
1	0	0	0	TTLTRG0
1	0	0	1	TTLTRG1
1	0	1	0	TTLTRG2
1	0	1	1	TTLTRG3
1	1	0	0	Channel 1 TRIGB
1	1	0	1	Channel 2 TRIGB
1	1	1	0	Channel 3 TRIGB
1	1	1	1	Channel 4 TRIGB
0	X	X	X	Disabled

TRIGB — These bits select the TRIGB routing according to the table below:

Bit 3	Bit 2	Bit 1	Bit 0	TRIGB Routing
1	0	0	0	TTLTRG4
1	0	0	1	TTLTRG5
1	0	1	0	TTLTRG6
1	0	1	1	TTLTRG7
1	1	0	0	Channel 1 TRIGA
1	1	0	1	Channel 2 TRIGA
1	1	1	0	Channel 3 TRIGA
1	1	1	1	Channel 4 TRIGA
0	X	X	X	Disabled

1.10 COND Register

Each 2108 channel can generate an interrupt on the VXI backplane. This register contains the current state/condition of the status bits that can be programmed to generate the interrupt.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU													PTM	TB	CI

Field/Bit Description:

CI	A logic high on this bit indicates that a channel interrupt event has occurred.
TB	A logic high on this bit indicates that the output trigger (TRIGB) is high.
PTM	A logic high on this bit indicates a voltage or temperature failure.

1.11 PTE Register

Each 2108 channel can generate an interrupt on the VXI backplane. This register allows the user to enable a low to high transition on a status bit to generate an interrupt event.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU													PTM	TB	CI

Field/Bit Description:

CI	A logic high on this bit enables the low to high transition of the channel interrupt status bit to signal an interrupt event.
TB	A logic high on this bit enables the low to high transition of the output trigger (TRIGB) status bit to signal an interrupt event.
PTM	A logic high on this bit enables the low to high transition of the power/temperature status bit to signal an interrupt event.

1.12 NTE Register

Each 2108 channel can generate an interrupt on the VXI backplane. This register allows the user to enable a high to low transition on a status bit to generate an interrupt event.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU													PTM	TB	CI

Field/Bit Description:

CI	A logic high on this bit enables the high to low transition of the channel interrupt status bit to signal an interrupt event.
TB	A logic high on this bit enables the high to low transition of the output trigger (TRIGB) status bit to signal an interrupt event.
PTM	A logic high on this bit enables the high to low transition of the power/temperature status bit to signal an interrupt event.

1.13 EVENT Register

Each 2108 channel can generate an interrupt on the VXI backplane. This register allows the user to read which status bit has transitioned to generate an interrupt event.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU													PTM	TB	CI

Field/Bit Description:

CI	A logic high on this bit indicates a channel interrupt status bit transition.
TB	A logic high on this bit indicates a output trigger (TRIGB) status bit transition.
PTM	A logic high on this bit indicates a power/temperature status bit transition.

Notes:

1. A read clears the entire event register.

1.14 ENABLE Register

Each 2108 channel can generate an interrupt on the VXI backplane. This register allows the user to enable/disable status bits to generate an interrupt event.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU													PTM	TB	CI

Field/Bit Description:

CI	A logic high on this bit enables the channel interrupt event to generate a VXI interrupt.
TB	A logic high on this bit enables the trigger output event to generate a VXI interrupt.
PTM	A logic high on this bit enables the power/temperature event to generate a VXI interrupt.

1.15 INTR Register

This register returns the selected interrupt level setting.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU													LEVEL		

Field/Bit Description:

LEVEL — These bits return the interrupt signal selected:

Bit 2	Bit 1	Bit 0	Interrupt Level
0	0	0	Disabled
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

1.16 PWR/TEMP Register

This register returns the temperature/voltage status.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU	T4	T3	T2	T1	NU	V10	V9	V8	V7	V6	V5	V4	V3	V2	V1

Field/Bit Description:

V1	Monitor for the +3.3V bus for channels one and two.
V2	Monitor for the +3.3V bus for channels three and four.
V3	Monitor for the -24V bus.
V4	Monitor for the -12V bus.
V5	Monitor for the +24V bus.
V6	Monitor for the +2.5V bus for channels one and two.
V7	Monitor for the +2.5V bus for channels three and four.
V8	Monitor for the -5.2V bus.
V9	Monitor for the -2V bus.
V10	Monitor for the +12V bus.
T1	Monitor for channel one temperature.
T2	Monitor for channel two temperature.
T3	Monitor for channel three temperature.
T4	Monitor for channel four temperature.

Notes:

1. A one indicates an error.

1.17 PAGE Register

This register controls the A24 memory page.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU							MAP	A21	NU						

Field/Bit Description:

A21 — If the 2108 is set to A24 mode and map mode is active then this bit controls the level of A21 during VXI read/write operation.

MAP — This bit indicates the state of the map mode (0 = map mode not active, 1 = active), see note 1.

Notes:

1. Read only bit.

2 2108 Baseboard A24/32 Map

The 2108 baseboard A24/A32 address space is used to program/query the reference signals used by the interconnect modules.

The baseboard A24/32 memory base address is 100000h and is segmented into register areas described below:

Register Segment Code (RSC)				Register Segment Name	Offset 100000h + RSC	Description
A18	A17	A16	A15			
0	0	1	1	REF	118000h	Reference Data Register
0	1	0	0	REFCS	120000h	Reference Control/Status Register

Table B-2 Baseboard A24/A32 Register List

2.1 Reference Data Registers (REF,W:118000_h - 118010_h)

These registers allows the user to program the reference signals baseboard. The table below shows the address assignment of each reference.

Address	Reference	Transmitter Function	Receiver Function
118000_h	0	VOHA	GOOD1REF (RxData)
118002_h	1	VOLA	GOOD0REF (RxData)
118004_h	2	VISRA	GOOD1REF (RxClkIn2)
118006_h	3	VOHB	GOOD1REF (RxQual1)
118008_h	4	VOLB	GOOD1REF (RxQual2)
$11800A_h$	5	VISRB	NU
$11800C_h$	6	VOZ1	NU
$11800E_h$	7	VOZ2	NU
118010_h	8	GOOD1REF (TxClkIn2)	NU

Table B-3 lists the bit definitions of the reference data register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU								DATA							

Table B-3 Reference Data Register Bit Description

Field Bit Definition:

DATA — Data to be written to the reference logic (reference and voltage).

Notes:

1. Programming the reference voltages is performed by writing three bytes to the PIC controller that maintains the reference voltages using phase width modulation (PWM). The three bytes are described below:

Byte	Data
0	Reference
1	Voltage (MSB)
2	Voltage (LSB)

Byte 0 determines which one of the 9 reference to program.

Byte 1 and Byte 2 form a 16 bit voltage word.

Byte 1 and 2 are calculated using the following formula:

$V_{word} = V / 0.10$

Where V_{word} = 16 bit voltage word and V = desired reference voltage in volts.

For example if the user wants VIH2 = 3.25V then:

$V_{word} = 3.25 / 0.01 = 325 = 145_{16}$

Byte 0 = 7

Byte 1 = 1

Byte 2 = 45_{16}

2. After each byte the “BUSY” bit in the control/status register below will go high until the reference logic is ready for the next byte.

2.2 Reference Control/Status Register (REFCS, RW:120000_h)

The reference control/status register allows the user to program the reference signals.

Table B-4 lists the bit description of the data formatter/status register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
													RST	BUSY	FLT

Table B-4 Reference Control/Status Bit Description

Field Bit Definition:

FLT	Reference fault flag (1 = reference fault, 0 = no reference fault).
BUSY	Reference busy flag (1 = busy, 0 = not busy).
RST	Reference reset (1 = enabled, 0 = disabled).

Notes:

1. FLT occurs when the reference cannot reach its programed level. The FLT flag is reset by writing a zero to bit 0.
2. The BSY flag indicates when the reference logic is ready for the next data byte.
3. A 1 written to the RST bit initiates a reset function which sets all the references to zero. The RST bit will go low when the reset function is complete.

3 2108Tx Register Map

The 2108Tx uses the upper three address bits (A21, A20, A19) to define four major segments.

Table B-7 below lists the major segments.

Major Segment Code			Major Segment Name	Offset	Description
A21	A20	A19			
0	0	0	BSREG	0h	Bit slice registers.
0	0	1	DFREG	80000h	Data formatter registers.
0	1	0	IFCREG	100000h	Interface registers.
1	X	X	CMTDATA	200000h	Command Memory Table data.

Table B-7 Model 2108 Transmitter Segment Address Map

Each major segment is further divided into register segments by the next four address bits (A18, A17, A16, A15).

3.1 Bit Slice Register Description (BSREG)

The bit slice register segments are described below:

Register Segment Code (RSC)				Register Segment Name	Offset BSREG + RSC	Description
A18	A17	A16	A15			
0	0	0	0	TVXIREG	0h	VXI Register Memory
0	0	0	1	BSCMD	8000h	Bit Slice Command
0	0	1	0	SUB	10000h	Subroutine Registers
0	0	1	1	SCMD	18000h	Synchronous Command Registers
0	1	1	0	BSINTR	30000h	Interrupt Control Registers
0	1	1	1	CONTROL	38000h	Control registers
1	1	1	1	BSREV	78000h	BS Revision

Table B-6 Bit Slice Register Segments

The following sections describes the registers of the Bit Slice memory.

3.1.1 VXI Register Memory (TVXIREG,R:0_h)

This register contains the VXI A16 ID and DEVICE register data for the 2108 transmitter module. Table B-5 lists the bit definitions of the VXI register.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Device Type																ID															

Table B-5 VXI Register Bit Definition

Field Bit Definition:

ID — VXI ID register. ($DF0F_h$)
Device Type — VXI Device Type Register. (9110_h)

Notes:

None

3.1.2 Bit Slice Command Memory (BSCMD,R/W:8000_h)

The bit slice memory is used to program and execute the Data Formatter.

The bit slice memory is stored in an array of 1024 long words illustrated below.

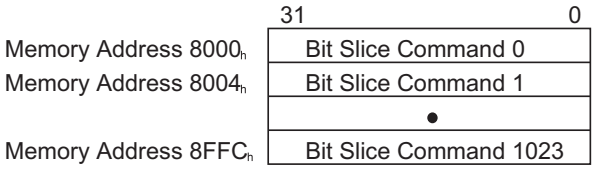


Figure B-1 Bit Slice Command Memory Addressing

Table B-8 lists the bit definitions of the bit slice command memory.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC				SC				Parameters																							

Table B-8 Bit Slice Bit Definition

Field/Bit Definition:

Parameters — The parameter field contents are based on the command type and are documented in the following sections.

SC — This field is used to segment command types.

OC — This field is used to specify the command type.

Bit 31	Bit 30	Bit 29	Bit 28	Operation
0	0	0	0	SET WORD COUNT
0	0	0	1	TRANSMIT
0	1	1	0	DEFINE
0	1	1	1	SET CONTROLS
1	0	1	0	REPEAT
1	1	1	0	NOP
1	1	1	1	JUMP

Notes:

None

3.1.2.1 "SET WORD COUNT"

This command programs the CMT (Command Memory Table) word count.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				SC				NU					WORD CNT																		

Field/Bit Definition:

WORD CNT — Word count. (1 to 512K)

SC — This selects which word count register is set. (0 - "IDLE", 1 - Normal)

Notes:

None

3.1.2.2 "TRANSMIT CMT"

This command enables a CMT to be transmitted by the 2108.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1				SC				PR	NU	P		MEM	MEM ADDR																		

Field/Bit Definition:

MEM ADDR — Starting address of the CMT. (0 to $3FFFF_h$)
MEM — CMT bank select. (0 = Bank A, 1 = Bank B)
P — CMT parity control.

Bit 21	Bit 20	Parity Control
0	0	Stop parity, hold current value
0	1	Start odd parity
1	0	Start even parity
1	1	Resume

PR — PRBS re-seed. (1 = reseed)
SC — This field selects the transmit command defined below:

Bit 27	Bit 26	Bit 25	Bit 24	Transmit Command
0	0	0	0	Transmit IDLE CMT
0	0	0	1	Transmit Normal CMT
0	0	1	0	Resume Normal CMT
0	0	1	1	NU
0	1	0	0	Transmit “IDLE” one word
0	1	0	1	Transmit Normal one word
0	1	1	0	Resume Normal one word
0	1	1	1	NU

Notes:

1. The CMT length is defined by the “SET WORD COUNT” command.
2. The accumulated parity is appended when the “AP” bit in the CMT is set, refer to section TBS.
3. Refer to section TBS for setting the PRBS seed value.

3.1.2.3 “DEFINE”

This command programs the loop, flag and receiver control registers.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
6				SC				NU								PARAMETERS															

Field/Bit Definition:

PARAMETERS — Data value for the selected register.
SC — Register select code.

Bit 27	Bit 26	Bit 25	Bit 24	Selected Register
0	0	0	0	Loop counter zero (L0)
0	0	0	1	Loop counter one (L1)
0	0	1	0	Loop counter two (L2)
0	0	1	1	Loop counter three (L3)
0	1	0	0	Front panel flags
0	1	0	1	General Purpose flags
0	1	1	1	Receiver flags

3.1.2.3.1 Define Loop Counter

This command allows the bit slice to program a loop count in one of the four loop counters.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
6				SC				NU								VALUE															

Field/Bit Definition:

VALUE — Loop count for selected counter. (1 to $FFFF_h$)
SC — Loop counter number to define. (0 to 3)

Notes:

None

3.1.2.3.2 Define Front Panel Output Flags (TxFLAGOUT1/TxFLAGOUT2)

This command allows the bit slice to program the front panel output flags.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
6				4				NU								MASK				DRVEN				Reserved (0)				LEVEL			

Field/Bit Definition:

LEVEL — Level for selected flag.

Bit 3	Bit 2	Bit 1	Bit 0	Bit Definition
Reserved (0)		TxFLAGOUT2	TxFLAGOUT1	1 = Logic “1”, 0 = Logic “0”

DRVEN — Driver enable for the selected flag.

Bit 11	Bit 10	Bit 9	Bit 8	Bit Definition
Reserved (0)		TxFLAGOUT2	TxFLAGOUT1	1 = Enabled , 0 = Disabled

MASK — Update mask to enable or disable DRVEN and LEVEL changes for the selected flag.

Bit 15	Bit 14	Bit 13	Bit 12	Bit Definition
Reserved (0)		TxFLAGOUT2	TxFLAGOUT1	1 = Update, 0 = No change

Notes:

None

3.1.2.3.3 Define General Purpose Output Flags (GPO1/GPO2)

This command allows the bit slice to program the general purpose output flags.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
6				5				NU								MASK				DRVEN				Reserved (0)				LEVEL			

Field/Bit Definition:

LEVEL — Level for selected flag.

Bit 3	Bit 2	Bit 1	Bit 0	Bit Definition
Reserved (0)		GPO2	GPO1	1 = Logic “1”, 0 = Logic “0”

DRVEN — Driver enable for the selected flag.

Bit 11	Bit 10	Bit 9	Bit 8	Bit Definition
Reserved (0)		GPO2	GPO1	1 = Enabled , 0 = Disabled

MASK — Update mask to enable or disable DRVEN and LEVEL changes for the selected flag.

Bit 15	Bit 14	Bit 13	Bit 12	Bit Definition
Reserved (0)		GPO2	GPO1	1 = Update, 0 = No change

Notes:

1. The general purpose output flags can be queried by the bit slice (section TBS) or the VXI Slot 0 controller (section TBS).
2. The general purpose output flags can be routed to the VXI TTLTRG bus (section TBS) as well as the interrupt logic (section TBS).

3.1.2.3.4 Define Receiver Control Flags (R-MODECTRL, R-CMDNUM0-3)

This command allows the bit slice to program the receiver flags.

After the level of the flags are set then a “STARTCMD” pulse will be generated.

Bit #																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
6				7				NU																			LEVEL				

Field/Bit Definition:

LEVEL — Level for selected flag.

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit Definition
MODECTRL	CMDNUM3	CMDNUM2	CMDNUM1	CMDNUM0	1 = Logic “1”, 0 = Logic “0”

Notes:

1. The “MODECTRL” flag sets the receiver run mode, 1 = Single, 0 = Multiple.
2. “CMDNUM0” through “CMDNUM3” are used when “MODECTRL” is set to 0 and they define the trigger command to run.

3.1.2.4 “SET CONTROLS” Command

This command is used to stop transmitter execution as well as requesting bank memory access.

Bit #																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7				SC				NU																							

Field/Bit Definition:

SC — Control command.

Bit 27	Bit 26	Bit 25	Bit 24	Selected Register
0	0	0	0	Request CMT bank memory “A”
0	0	0	1	Request CMT bank memory “B”
0	0	1	0	Release CMT bank memory “A”
0	0	1	1	Release CMT bank memory “B”
0	1	0	0	HALT CMT Sequence

Notes:

1. “HALT”ing the CMT sequence returns to the “IDLE” CMT.

3.1.2.5 “REPEAT NEXT” Command

This command enables a non-jump command to be repeated up to 512K times.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A_h				0				NU					REPEAT																		

Field/Bit Definition:

REPEAT Repeat count. (1 to $3FFFF_h$)

Notes:

None

3.1.2.6 "JUMP" Command

The jump command allows the user to control the bit slice program flow.
There are several test conditions described below and in the following sections.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F_h				SC				NU								PARAMETERS															

Field/Bit Definition:

PARAMETERS Jump parameters.
SC Jump test condition.

Bit 27	Bit 26	Bit 25	Bit 24	Jump Condition
0	0	0	0	NONE (Unconditional Jump)
0	0	0	1	Loop Counter State
0	0	1	0	Front Panel Flag Status
0	0	1	1	General Purpose Flag Status
0	1	0	0	Receiver Flag Status
0	1	0	1	Tx/Rx Busy Flag Status
0	1	1	0	Bank Memory Grant Flag Status
0	1	1	1	Bank Memory Full Status
1	1	1	0	Jump Breakpoint
1	1	1	1	Jump Return

PARAMETERS Jump command parameters.

Notes:

None

3.1.2.6.1 None (Unconditional)

Jump to a new bit slice address.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F_h				0_h				NU								SUB	NU					ADDR									

Field/Bit Definition:

ADDR Jump to address.
SUB Return flag. (1 = Save Return Address, 0 = Don't save)

Notes:

None

3.1.2.6.2 Loop Counter

Test the loop counter and jump if equal or not equal to one. Each subroutine level has four loop counters
The specified loop counter is decremented after the test is performed.

Bit #																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F_h				1_h				NU								SUB	T/F	CNT		NU		ADDR									

Field/Bit Definition:

ADDR Jump to address.

CNT Counter number to test.

Bit 13	Bit 12	Counter
0	0	0
0	1	1
1	0	2
1	1	3

T/F True/False Flag. (0 = Jump if counter not equal to one “FALSE”, 1 = Jump if counter equal one “TRUE”.)

SUB Return flag. (1 = Save Return Address, 0 = Don’t save)

Notes:

None

3.1.2.6.3 Front Panel Flag

Test the front panel flag and jump if high, low, rising edge or falling edge.

Bit #																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F_h				2_h				NU						TC		SUB	NU	FLAG		NU		ADDR									

Field/Bit Definition:

ADDR Jump to address.

FLAG Flag number to test.

Bit 13	Bit 12	Flag
0	0	TxFLAGOUT1
0	1	TxFLAGOUT2
1	0	TxFLAGIN1
1	1	TxFLAGIN2

SUB Return flag. (1 = Save Return Address, 0 = Don’t save)

TC Test Code

Bit 17	Bit 16	Test Code
0	0	Test for Low Level
0	1	Test for High Level
1	0	Test for Falling Edge
1	1	Test for Rising Edge

Notes:

None

3.1.2.6.4 Event Flag

Test the event flags and jump high, low, rising edge or falling edge.

Bit #																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F_h				3_h				NU						TC		SUB	FLAG			NU	JA	ADDR									
																						JAR									

Field/Bit Definition:

JVEC — Jump Address Register programmed by the CPU.
ADDR — Jump to address.
JA — Jump to Location. (0 = ADDR, 1 = Jump Address Register “JAR”, section 3.1.4.9)
FLAG — Flag number to test.

Bit 14	Bit 13	Bit 12	Flag
0	0	0	GPO1
0	0	1	GPO2
0	1	0	GPI1
0	1	1	GPI2
1	0	0	TRIGA
1	0	1	Sync Pulse
1	1	0	Replace Data Compare
1	1	1	Bit Slice Address Compare

SUB — Return flag. (1 = Save Return Address, 0 = Don’t save)
TC — Test Code

Bit 17	Bit 16	Test Code
0	0	Test for Low Level
0	1	Test for High Level
1	0	Test for Falling Edge
1	1	Test for Rising Edge

Notes:

None

3.1.2.6.5 Receiver Flag

Test the receiver trigger flag (RxTRIGVALID) and jump if true/false.

Bit #																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F_h				4_h				NU								SUB	T/F	NU			JA	ADDR									
																						ADDR[9:4]						RxTRIGNUM			

Field/Bit Definition:

RxTRIGNUM — Receiver Trigger number.
ADDR[9:4] — Upper six bits of ADDR.
ADDR — Jump to address.
JA — Jump to Location. (0 = “ADDR”, 1 = 6 MSBs of ADDR + 4 LSBs from receiver TRIGNUM)
T/F — True/False Flag. (0 = Jump if False, 1 = Jump if True)
SUB — Return flag. (1 = Save Return Address, 0 = Don’t save)

Notes:

None

3.1.2.6.6 Busy Flag

Test the transmitter and receiver busy flags and jump if true/false.

Bit #																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F_h				5_h				NU								SUB	T/F	NU	TR	NU		ADDR									

Field/Bit Definition:

ADDR — Jump to address.
TR — Transmit/Receive (0 = Receiver busy flag, 1 = Transmitter busy flag)

T/F	True/False Flag. (0 = Jump if False, not busy, 1 = Jump if True, busy)
SUB	Return flag. (1 = Save Return Address, 0 = Don't save)

Notes:

None

3.1.2.6.7 Command Memory Status

Test the command memory status and jump if true/false.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F_h				SC				NU								SUB	T/F	NU	MEM	NU		ADDR									

Field/Bit Definition:

ADDR	Jump to address.
MEM	Memory to test. (0 = Bank "A", 1 = Bank "B")
T/F	True/False Flag. (0 = Jump if False, 1 = Jump if True)
SUB	Return flag. (1 = Save Return Address, 0 = Don't save)
SC	Status select (6 = memory grant, 7 = memory full)

Notes:

None

3.1.2.6.8 Self

Jump to current address and force a breakpoint condition.

Bit #-																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F_h				E_h				NU																							

3.1.2.6.9 Subroutine Return

Jump to the last address in the saved from a previous "JUMP" command.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F_h				F_h				NU																							

3.1.3 Subroutine Registers (SUB)

This memory contains the bit slice subroutine status and stack information.

3.1.3.1 Subroutine Status Register (SUBSTAT,R:10000_h)

This register returns the subroutine status.

Table B-9 lists the bit description of the subroutine status register.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU						PADDR										SCNT				NU	SA	RADDR									

Table B-9 Subroutine Status Register Bit Definition

Field/Bit Definition:

RADDR	Current subroutine return address.

SA	Subroutine Active Flag (1 = Active subroutine, 0 = No subroutine (SCNT = 0) or overflow (SCNT = 15).
SCNT	Subroutine Count
PADDR	Current Bit Slice Address.

Notes:

None

3.1.3.2 Subroutine Memory (SUBMEM,R:10040_h)

The subroutine memory stores the subroutine stack data.

Figure B-2 illustrates the address mapping of the subroutine memory

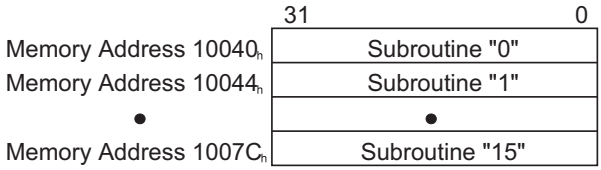


Figure B-2 Subroutine Memory Addressing

Table B-9 lists the bit description of the subroutine memory.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU						PADDR										SCNT				NU	SA	RADDR									

Table B-11 Subroutine Memory Bit Definition

Field/Bit Definition:

RADDR	Current subroutine return address.
SA	Subroutine Active Flag (1 = Active subroutine, 0 = No subroutine (SCNT = 0) or overflow (SCNT = 15).
SCNT	Subroutine Count
PADDR	Current Bit Slice Address.

Notes:

None

3.1.4 Synchronous Command Registers (SCMD)

The synchronous command registers are clocked by the bit slice clock and described below:

Register Code						Name	Offset	Description
A5	A4	A3	A2	A1	A0			
0	0	0	1	X	X	BSA0	18004h	Bit Slice Address Zero
0	0	1	0	X	X	ACR	18008h	Alternate Command Register
0	0	1	1	X	X	RDCMP	1800Ch	Replace Data Compare Address
0	1	0	0	X	X	SPCADDR	18010h	Sync Pulse Compare Address
0	1	0	1	X	X	ACRCMP	18014h	Alternate Command Register Compare
0	1	1	0	X	X	GPFWRT	18018h	General Purpose Flag Write
0	1	1	1	X	X	MEMCTRL	1801Ch	Memory Control
1	0	0	0	X	X	RSTCTRL	18020h	Reset Control
1	0	0	1	X	X	JAR	18024h	Jump Address Register

Table B-10 Synchronous Command Registers

The following sections describes the synchronous command registers.

3.1.4.1 Bit Slice Address Zero Register (BSA0,W:18004_h)

A write to this register forces the Bit Slice Address to zero.

3.1.4.2 Alternate Command Register (ACR,R/W:18008_h)

The alternate command register allows the user to substitute a bit slice command to be executed.

The substituted bit slice command is programmed in this register (see section 3.1.2 of this appendix) and is enabled by programming ACRCMP register, section 1.1.4.53.1.4.5.

3.1.4.3 Replace Data Compare (RDCMP,R/W:$1800C_h$)

This register allows the user to set and enable a compare address that will generate a compare signal to the data formatter. The data formatter will substitute the contents of the bank memory with the contents of the replace register (REPREG, section 3.2.4)

Table B-13 lists the bit description of the replace data compare memory

Bit #																												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU											ENB	ENA	COMPARE ADDR																	

Table B-13 Replace Data Compare Bit Definition

Field/Bit Definition:

COMPARE ADDR	Bank memory address to compare.
ENA	Enable compare bank A (1 = enabled, 0 = disabled).
ENB	Enable compare bank B (1 = enabled, 0 = disabled).

Notes:

None

3.1.4.4 Sync Pulse Compare (SPCMP,R/W:18010_h)

This register allows the user to set and enable a compare address that will generate a “TxSYNCPULSE” signal to the front panel. The data formatter controls the width of the sync pulse through the output control register (section 3.2.5.1).

Table B-12 lists the bit description of the sync pulse compare register.

Bit #																												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU											ENB	ENA	COMPARE ADDR																	

Table B-12 Sync Pulse Compare Bit Definition

Field/Bit Definition:

COMPARE ADDR	Bank memory address to compare.
ENA	Enable compare bank A (1 = enabled, 0 = disabled).
ENB	Enable compare bank B (1 = enabled, 0 = disabled).

Notes:

None

3.1.4.5 Alternate Command Register Compare (ACRCMP,R/W:18014$_h$)

This register allows the user to set and enable a compare address that will cause the bit slice command programmed in the ACR register (section 3.1.4.2) to be substituted with the bit slice command at the specified address. The ACR can also be substituted immediately.

Table B-15 lists the bit description of the replace data compare register.

Bit #																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU																			FORCE	BPHALT	EN	COMPARE ADDR									

Table B-15 Alternate Command Register Bit Definition

Field/Bit Definition:

COMPARE ADDR	Bit slice memory address to compare.
EN	Enable the ACR compare (1 = enabled, 0 = disabled).
BPHALT	Halt if the ACR is a “JUMP BREAKPOINT” command (1 = halt, 0 = do not halt). Re-programming this register causes the bit slice command at the specified address to be executed.
FORCE	Force the ACR until disabled (1 = force enabled, 0 = force disabled).

Notes:

1. EN bit is reset after compare execution.

3.1.4.6 Flag Status (GPFWRT,W:18018$_h$)

This register allows the user to program the level of the general purpose flags.

Table B-14 lists the bit description of the general purpose flag register.

Bit #																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU																														LEV

Table B-14 General Purpose Flag Bit Definition

Field/Bit Definition:

LEV General purpose flag level (0 = low, 1 = high).

Bit 1	Bit 0
GPO2	GPO1

Notes:

None

3.1.4.7 Memory Control (MEMCTRL,W:1801C$_h$)

This register allows the user to request and release bank memory. Bank memory status is read through the BSSTAT register (section 3.1.6.2).

Table B-17 lists the bit description of the memory control register.

Bit #																												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU																			REMAP	BE3	BE2	BE1	BE0	RSTB	RELB	BFULL	REQB	RSTA	RELA	AFULL	REQA

Table B-17 Memory Control Bit Definition

Field/Bit Definition:

REQA	Request bank “A” memory (1 = request memory, 0 = don’t request).
AFULL	Set the bank “A” full flag (1 = set flag, 0 = don’t set flag).
RELA	Release bank “A” memory (1 = release, 0 = don’t release).
RSTA	Reset bank “A” request and bank “A” full bits.
REQB	Request bank “B” memory (1 = request memory, 0 = don’t request).
BFULL	Set the bank “B” full flag (1 = set flag, 0 = don’t set flag).
RELB	Release bank “B” memory (1 = release, 0 = don’t release).
RSTB	Reset bank “B” request and bank “B” full bits.
BE0	Bank memory D7 through D0 mask (1 = enabled, 0 = masked).
BE1	Bank memory D15 through D8 mask (1 = enabled, 0 = masked).
BE2	Bank memory D23 through D16 mask (1 = enabled, 0 = masked).
BE3	Bank memory D31 through D24 mask (1 = enabled, 0 = masked).
REMAP	Remap CMT memory for D16 transfers (1 = enabled, 0 = disabled).

Notes:

None

3.1.4.8 Reset Control (RSTCTRL,W:18020_h)

This register allows the user to reset bit slice functions defined below.

Table B-16 lists the bit description of the reset control register.

Bit #																												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU																	RSTO	RSTN	RSTM	RSTL	RSTK	RSTJ	RSTI	RSTH	RSTG	RSTF	RSTE	RSTD	RSTC	RSTB	RSTA

Table B-16 Reset Control Bit Definition

Field/Bit Definition:

RSTA	Reset loop and repeat counters to done.
RSTB	Reset “LASTBYTE” to stop current stream.
RSTC	Reset subroutine address to zero.
RSTD	Reset “SERR” and “MEMERR”
RSTE	Reset general purpose flags.
RSTF	Reset front panel flags.
RSTG	Reset receiver control signals.
RSTH	Reset jump logic.
RSTI	Reset “ACR” flag, note 1.
RSTJ	Set “ACR” flag, note 1.
RSTK	Reset “ACR” to “JUMP SELF”
RSTL	Reset bank “A” memory arbitration.
RSTM	Reset bank “B” memory arbitration.
RSTN	Reset trigger, out and receiver.
RSTO	Reset IRQ registers.

Notes:

1. Do not program at same time.

3.1.4.9 Jump Address Register (JAR,R/W:18024$_h$)

This register allows the user to program jump address register.

Table B-20 lists the bit description of the jump address register.

Bit #																											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU																		TTNUM				JVEC									

Table B-20 Jump Address Bit Definition

Field/Bit Definition:

JVEC — Jump vector used with the “JUMP GENERAL PURPOSE FLAG” bit slice command, read/write.

TTNUM — Transmitter trigger number, read only.

Bit 13	Bit 12	Bit 11	Bit 10
TxTRIGNUM3	TxTRIGNUM2	TxTRIGNUM1	TxTRIGNUM0

Notes:

None

3.1.5 Bit Slice Interrupt Control Registers (BSINTR)

The interrupt control registers allow the user to map and enable interrupt generation.

The control registers are mapped as described below.

Address LSB					Name	Offset	Description
A4	A3	A2	A1	A0			
0	0	0	X	X	BSPTE	30000h	Positive Transition Enable
0	0	1	X	X	BSNTE	30004h	Negative Transition Enable
0	1	0	X	X	BSIRQEN	30008h	Interrupt Enable
0	1	1	X	X	BSINT	3000Ch	Interrupt Register
1	0	0	X	X	BSEVENT	30010h	Event Register

Table B-18 Interrupt Control Registers

3.1.5.1 Bit Slice Positive Transition Enable (BSPTE:30000$_h$)

This register allows the user to program the event mask register for events going low to high.

Table B-19 lists the bit description of the positive transition enable register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU									BSGB	BSGA	TRIGB	TRIGA	SERR	MERR	NOCLK

Table B-19 Bit Slice Positive Transition Enable Bit Definition

Field/Bit Definition:

NOCLK — No Clock; Slow or missing clock.

MERR — Memory Error;

SERR — Subroutine Error;

TRIGA — Trigger A Input.

TRIGB — Trigger B Output;

BSGA	Bit Slice Grant Bank A;
BSGB	Bit Slice Grant Bank B;

Notes:

1. 0 = disable positive event transition, 1 = enable event on low to high transition.

3.1.5.2 Bit Slice Negative Transition Enable (BSNTE:30004$_h$)

This register allows the user to program the event mask register for events going negative.
Table B-22 lists the bit description of the negative transition enable register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU									BSGB	BSGA	TRIGB	TRIGA	SERR	MERR	NOCLK

Table B-22 Bit Slice Negative Transition Enable

Field/Bit Definition:

NOCLK	No Clock; Slow or missing clock.
MERR	Memory Error;
SERR	Subroutine Error;
TRIGA	Trigger A Input.
TRIGB	Trigger B Output;
BSGA	Bit Slice Grant Bank A;
BSGB	Bit Slice Grant Bank B;

Notes:

1. 0 = disable negative event transition, 1 = enable event on high to low transition

3.1.5.3 Bit Slice Interrupt Event Enable Register (BSIRQEN:30008$_h$)

This register allows the user to program specific event to cause an interrupt.
Table B-21 lists the bit description of the event enable register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU									BSGB	BSGA	TRIGB	TRIGA	SERR	MERR	NOCLK

Table B-21 Bit Slice Interrupt Event Enable Register Bit Definition

Field/Bit Definition:

NOCLK	No Clock; Slow or missing clock.
MERR	Memory Error;
SERR	Subroutine Error;
TRIGA	Trigger A Input.
TRIGB	Trigger B Output;
BSGA	Bit Slice Grant Bank A;
BSGB	Bit Slice Grant Bank B;

Notes:

1. 0 = disable event interrupt, 1 = enable event interrupt

3.1.5.4 Interrupt Register (BSINT:3000C$_h$)

This register allows the user to query the current status of the interrupt bits.

Table B-24 lists the bit description of the event enable register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU									BSGB	BSGA	TRIGB	TRIGA	SERR	MERR	NOCLK

Table B-24 Interrupt Register Bit Definitions

Field/Bit Definition:

NOCLK	No Clock; 1 = slow or missing clock.
MERR	Memory Error; 1 = attempt to transmit a memory bank that is not released.
SERR	Subroutine Error; 1 = subroutine stack overflow or return with no subroutine.
TRIGA	Trigger A Input; Level of the selected input signal.
TRIGB	Trigger B Output; Level of the selected output signal.
BSGA	Bit Slice Grant Bank A; 1 = Bit Slice owns bank A memory.
BSGB	Bit Slice Grant Bank B; 1 = Bit Slice owns bank B memory.

Notes:

None

3.1.5.5 Bit Slice Interrupt Event Register (BSEVENT:30010_h)

This register allows the user to query the interrupt event status. This register is cleared after it is queried. Table B-23 lists the bit description of the interrupt event register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU									BSGB	BSGA	TRIGB	TRIGA	SERR	MERR	NOCLK

Table B-23 Bit Slice Interrupt Event Register Bit Definition

Field/Bit Definition:

NOCLK	No Clock; Slow or missing clock.
MERR	Memory Error;
SERR	Subroutine Error;
TRIGA	Trigger A Input.
TRIGB	Trigger B Output;
BSGA	Bit Slice Grant Bank A;
BSGB	Bit Slice Grant Bank B;

Notes:

1. 1 = event true, 0 = event false.

3.1.6 Status/Control Registers (CONTROL)

The bit slice control registers are asynchronous, i.e., data formatter clocks are not required.

The control registers are mapped as described below.

Register Code						Name	Offset	Description
A5	A4	A3	A2	A1	A0			
0	0	0	0	X	X	ERROR	38000h	Error flags
0	0	0	1	X	X	BSSTAT	38004h	Bit Slice Status
0	0	1	0	X	X	DFSTAT	38008h	Packet Status
0	0	1	1	X	X	FLAG	3800Ch	Flag Status
0	1	0	0	X	X	LOOP01	38010h	Loop counter zero and one
0	1	0	1	X	X	LOOP23	38014h	Loop counter 2two and three
0	1	1	0	X	X	TTRIG	38018h	Trigger Control Register

Table B-27 Status/Control Registers

3.1.6.1 Error Flags (ERROR:38000_h)

This register allows the user to query bit slice error bits.

Table B-26 lists the bit description of the error register.

Bit #																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU																											CLK	MB	MA	RTN	SUB

Table B-26 Error Flags

Field/Bit Definition:

SUB	Subroutine error bit (1 = subroutine overflow, 0 = no error).
RTN	Return error (1 = return with no subroutine, 0 = no error).
MA	Execute stream bank “A” memory error (1 = attempt to execute bank “A” that is not released , 0 = no error).
MB	Execute stream bank “B” memory error (1 = attempt to execute bank “B” that is not released , 0 = no error)
CLK	Clock error (1 = No bit slice clocks, 0 = no error).

Notes:

None

Bits are reset by reading the register.

3.1.6.2 Bit Slice Status (BSSTAT:38004_h)

This register allows the user to query bit slice status bits.

Table B-25 lists the bit description of the bit slice status register.

Bit #																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TYPE				TBUSY	BSGB	FULLB	GRNTB	MSEL	BSGA	FULLA	GRNTA	AI	WORD COUNT																		

Table B-25 Bit Slice Status Bit Definition

Field/Bit Definition:

WORD COUNT	Current packet word count.
AI	Alternate instruction active (1 = active, 0 = not active).
GRNTA	User bank “A” grant (1 = User owns bank “A”, 0 = User released bank “A”).

FULLA Bank “A” memory full flag (1 = full, 0 = not full)
BSGA Bit slice bank “A” grant (1 = bit slice owns bank “A”, 0 = bit slice released bank “A”).
MSEL Current stream memory selected (0 = bank “A”, 1 = bank “B”).
GRNTB User bank “B” grant (1 = User owns bank “B”, 0 = User released bank “B”).
FULLB Bank “B” memory full flag (1 = full, 0 = not full)
BSGB Bit slice bank “B” grant (1 = bit slice owns bank “B”, 0 = bit slice released bank “B”).
TBUSY Transmitter busy flag (1 = stream active, 0 = stream not active).
TYPE Type bits for the current packet.

Bit 23	Bit 22	Bit 21	Bit 20	Type
0	0	0	0	Bank Memory
0	0	1	1	PRN 2^{32}-1
0	1	0	0	Random Delay
1	1	0	0	Fixed Delay

Notes:

None

3.1.6.3 Packet Status (DFSTAT,R:38008$_h$)

This register allows the user to query stream status bits.

Table B-29 lists the bit description of the stream status register.

Bit #																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU									BSRUN	RDCMP	SPCMP	IBUSY	PACKET ADDR																	

Table B-29 Packet Status Bit Definition

Field/Bit Definition:

PACKET ADDR Current stream address.
IBUSY Idle Busy (1 = idle state executed, 0 = not executed)
SPCMP Sync pulse compare flag (1 = compare true, 0 = compare not true).
RDCMP Replace data compare flag (1 = compare true, 0 = compare not true).
BSRUN Data formatter run request (1 = run request, 0 = not requested).

Notes:

None

3.1.6.4 Flag Status (FLAG,R:3800C$_h$)

This register allows the user to query flag status bits.

Table B-28 lists the bit description of the stream status register.

Bit #																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPFLAG				FPFLAG				RCNUM				RMODE	RSTRT	SCA	RPTA	RPTCNT															

Table B-28 Flag Status Bit Definition

Field/Bit Definition:

RPTCNT Current value of the repeat next counter.
RPTA Repeat Active bit. (0 = active, 1 = not active).

SCA Synchronous Command Active bit (1 = active, 0 = not active).
RSTRT RxSTARTCMD signal level.
RMODE RxMODECTRL signal level.
RCNUM RxCMDNUM bit levels.

Bit 23	Bit 22	Bit 21	Bit 20
RxCMDNUM3	RxRUNCODE2	RxRUNCODE1	RxRUNCODE0

FPFLAG Front panel flag level.

Bit 27	Bit 26	Bit 25	Bit 24
FLAG4 (TxFLAGIN2)	FLAG3 (TxFLAGIN1)	FLAG2 (TxFLAGOUT2)	FLAG1 (TxFLAGOUT1)

GPFLAG General purpose flag 3 level (0 = low, 1 = high).

Bit 31	Bit 30	Bit 29	Bit 28
GP3 (GPI2)	GP2 (GPI1)	GP1 (GPO2)	GP0 (GPO1)

Notes:

None

3.1.6.5 Read Loop Counter Zero/One (LOOP01,R:38010$_h$)

These registers allows the user to query the loop counter values for each subroutine level.
Table B-31 lists the addresses for each subroutine level.

Address	Subroutine Level
38010h	1
38030h	2
38050h	3
38070h	4
38090h	5
380B0h	6
380D0h	7
380F0h	8
38110h	9
38130h	10
38150h	11
38170h	12
38190h	13
381B0h	14
381D0h	15
381F0h	16

Table B-31 Loop Counter Zero/One Address Offset

Table B-30 lists the bit description of the loop counter zero/one register.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOOP1																LOOP0															

Table B-30 Loop Counter Zero/One Bit Definition

Field/Bit Definition:

LOOP 0 Current loop counter zero value.
LOOP 1 Current loop counter one value.

Notes:

None

3.1.6.6 Read Loop Counter Two/Three (LOOP23,R:38014$_h$)

This register allows the user to query the loop counter values.
Table B-34 lists the addresses for each subroutine level.

Address	Subroutine Level
38014h	1
38034h	2
38054h	3
38074h	4
38094h	5
380B4h	6
380D4h	7
380F4h	8
38114h	9
38134h	10
38154h	11
38174h	12
38194h	13
381B4h	14
381D4h	15

Table B-34 Loop Counter Two/Three Address Offset

Table B-33 lists the bit description of the loop counter two/three register.

Bit #																										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOOP3																LOOP2															

Table B-33 Loop Counter Two/Three Bit Definition

Field/Bit Definition:

LOOP 2 Current loop counter two value.
LOOP 3 Current loop counter three value.

Notes:

None

3.1.6.7 Trigger Control (TTRIG,R/W:38018$_h$)

This register allows the user to program the trigger and inter module control signals.
Table B-32 lists the bit description of the interrupt mask register.

Bit #																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU																								IME	AEN	TOE	NU	TOS			

Table B-32 Interrupt/Bank Memory Mask Bit Definition

Field/Bit Definition:

TOS Trigger Output Source.

Bit 11	Bit 10	Bit 9	Bit 8	Signal
0	0	0	0	General Purpose Flag 0 (GPO1)
0	0	0	1	General Purpose Flag 1 (GPO2)
0	0	1	0	General Purpose Flag 2 (GPI1)
0	0	1	1	General Purpose Flag 3 (GPI2)
0	1	0	0	Front Panel Flag 0 (TxFLAGOUT1)
0	1	0	1	Front Panel Flag 1 (TxFLAGOUT2)
0	1	1	0	Front Panel Flag 2 (TxFLAGIN1)
0	1	1	1	Front Panel Flag 3 (TxFALGIN2)
1	0	0	0	TxBUSY
1	0	0	1	TxSYNCPULSE
1	0	1	0	Replace Data Compare
1	0	1	1	Bit Slice Compare

TOE Trigger Output Enable. (1 = enabled, 0 = disabled).
AEN Acknowledge Enable. (1 = generate and enable TxACK handshake, 0 = disable).
IME Inter-module bus enable. (1 = enabled, 0 = disabled).

Notes:

1. Replace Data Compare, see section 1.1.4.33.1.4.3.
2. Bit Slice Compare, see section 1.1.4.53.1.4.5.

3.1.7 Bit Slice Revision (BSREV:78000_h)

This register allows the user to query the id and revision of the bit slice logic.

Table B-36 lists the bit description of the revision register.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MODEL																VER								REV							

Table B-36 Revision Register Bit Definition

Field/Bit Definition:

REV Revision code (TBD).
VER Version code (TBD).
MODEL Model code (TBD).

Notes:

None

3.2 Data Format Registers (DFREG:80000h)

The data formatter register segments are described below:

Register Segment Code (RSC)				Register Segment Name	Base Address DFREG + RSC	Description
A18	A17	A16	A15			
0	0	0	0	BFC	80000h	Bit Format Command Memory
0	0	0	1	DFR	88000h	Data Format Registers
0	0	1	0	WFR	90000h	Waveform Format Registers
0	0	1	1	REPREG	98000h	Replace Register
0	1	0	0	BFCTRL	A0000h	Bit Format Control Registers
0	1	0	1	DLYREG	A8000h	Fixed/Random Delay Registers
0	1	1	0	PRNSEED	B0000h	PRN Seed
0	1	1	1	TRUNREG	B8000h	Run/Stop register
1	0	0	0	DATA LUT	C0000h	Data Look Up Table
1	0	0	1	TCLKGEN	C8000h	Clock Generator Registers
1	0	1	0	TDCREG	D0000h	Output Delay Control Registers
1	1	1	0	DFINTR	F0000h	Interrupt Control Registers
1	1	1	1	DFREV	F8000h	DF Revision/Status

Table B-35 Data Format Memory

The following sections describes the register of the Data Format memory.

3.2.1 Bit Format Command (BFC:80000_h)

The bit format command registers are mapped as described below:

Register Code						Name	Offset	Description
A5	A4	A3	A2	A1	A0			
0	0	0	0	X	X	BFC1	80000h	Bit Format Command 1
0	0	0	1	X	X	BFC2	80004h	Bit Format Command 2
0	0	1	0	X	X	BFC3	80008h	Bit Format Command 3
0	0	1	1	X	X	BFC4	8000Ch	Bit Format Command 4
0	1	0	0	X	X	BFC5	80010h	Bit Format Command 5
0	1	0	1	X	X	BFC6	80014h	Bit Format Command 6
0	1	1	0	X	X	BFC7	80018h	Bit Format Command 7
0	1	1	1	X	X	BFC8	8001Ch	Bit Format Command 8
1	0	0	0	X	X	BFC9	80020h	Bit Format Command 9
1	0	0	1	X	X	BFC10	80024h	Bit Format Command 10
1	0	1	0	X	X	BFC11	80028h	Bit Format Command 11
1	0	1	1	X	X	BFC12	8002Ch	Bit Format Command 12
1	1	0	0	X	X	BFC13	80030h	Bit Format Command 13
1	1	0	1	X	X	BFC14	80034h	Bit Format Command 14
1	1	1	0	X	X	BFC15	80038h	Bit Format Command 15
1	1	1	1	X	X	BFC16	8003Ch	Bit Format Command 16

Table B-38 Bit Format Command Registers

The BFC registers contain the bit format commands for the “BIT FORMATTER” logic.
Each bit of the output data can select from one of sixteen bit format commands.
Table B-37 lists the bit definitions of the BFC memory.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ϕ2 Command								ϕ1 Command							

Table B-37 BFC Memory Definition

Field/Bit Definition:

ϕ1 Command — Phase 1 command.

Bit #							
7	6	5	4	3	2	1	0
RSEL	NU	STR	DE	BFCMD			

ϕ2 Command — Phase 2 command.

Bit #							
15	14	13	12	11	10	9	8
RSEL	NU	STR	DE	BFCMD			

BFCMD — Bit format command.
DE — Data enable bit (0 = HI-Z, 1 = enabled)
STR — Strobe Value (0 = logic zero, 1 = logic one)
RSEL — Reference Select (0 = Ref A, 1 = Ref B)

Notes:

1. The bit format command allows the user to specify a standard “Bit Format” such as RZ, AMI or BIPHASE-L (MANCHESTER) or program a user defined format.

2. The ϕ2 command is used in the one clock per bit mode.
3. Table B-39 lists the bit format commands.

Command	Value	Description	CB =	TV =
OBV	0_h	Output Bit Value	BV	TV
OCBV	1_h	Output Compliment Bit Value	$\overline{BV}$	TV
OLH	4_h	Output Logic High	Logic High	TV
OLL	5_h	Output Logic Low	Logic Low	TV
OPB	8_h	Output Previous Bit	PB	TV
OCPB	9_h	Output Compliment Previous Bit	$\overline{PB}$	TV
OPBS	A_h	Output Previous Bit if BV = Space	(BV=0)?PB (BV=1)?$\overline{PB}$	TV
OPBM	B_h	Output Previous Bit if BV = Mark	(BV=1)?PB (BV=0)?$\overline{PB}$	TV
OAMI	2_h	Output AMI	(BV=1)?$\overline{TV}$ (BV=0)?Z	(BV=1)?$\overline{TV}$ (BV=0)?TV
OAMIV	3_h	Output AMI Violation	(BV=1)?TV (BV=0)?Z	TV
CB = Current Bit, PB = Previous Bit, TV = Temp Value (AMI), Z = Logic Zero, BV = Bit Value				

Table B-39 Bit Format Command Listing

4. Figure B-3 illustrates the bit format commands used to implement common bit formats.

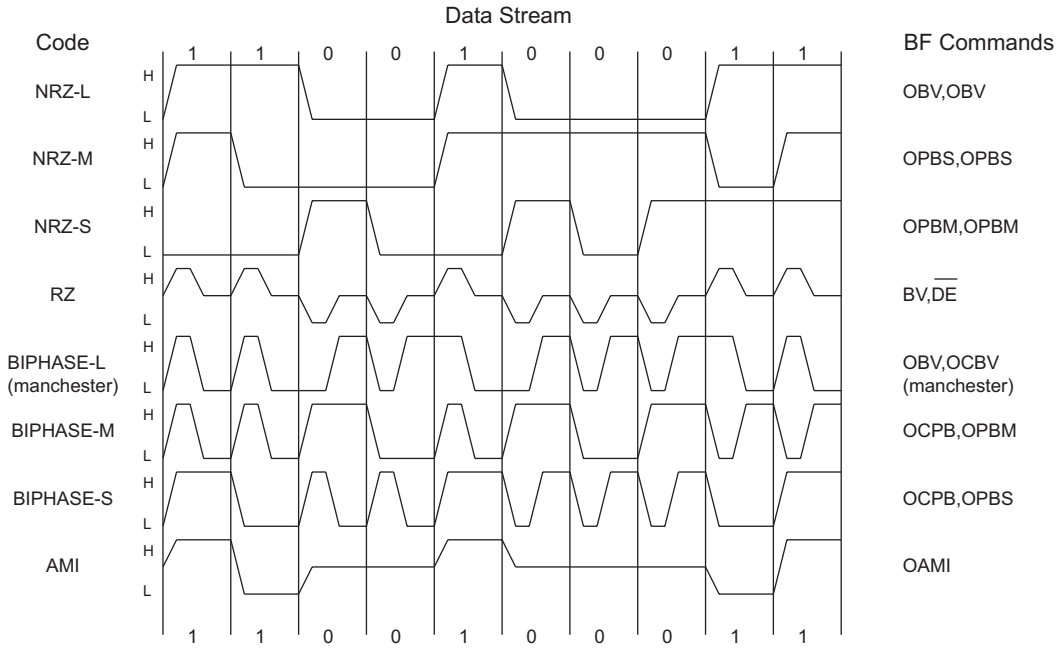


Figure B-3 Bit Format Command Examples

3.2.2 Data Format Registers (DFR:88000_h)

The DFR memory allows the operator to program sixteen data format registers. The data format registers contain indexes into the bit format memory as well as reference select compliment bit for every bit of the current “LUT DATA” field.

Figure B-5 illustrates the address mapping of the DFR memory.

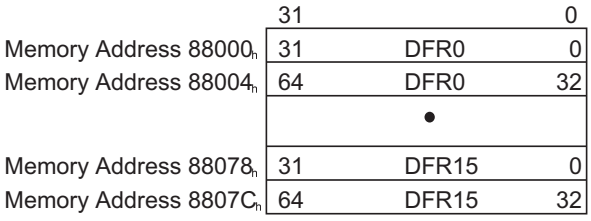


Figure B-5 DFR Memory Addressing

Table B-40 list the bit definitions of the DFR memory.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU	Bit 6 Format					Bit 5 Format					Bit 4 Format					NU	Bit 3 Format					Bit 2 Format					Bit 1 Format				

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
NU	Bit 12 Format					Bit 11 Format					Bit 10 Format					NU	Bit 9 Format					Bit 8 Format					Bit 7 Format				

Table B-40 DFR Memory Bit Definitions

Field/Bit Definition:

Bit n Format — Format for bit n.

Bit n Format				
4	3	2	1	0
CRSEL	BFI			

BFI — Bit Format Index (0 - 15).
CRSEL — Compliment the current RSEL setting (1 = compliment).

Notes:

None

3.2.3 Waveform Format Register (WFR:90000_h)

The waveform registers allows the user to input the shift count for each of the eight available waveforms. Figure B-4 illustrates the address mapping of the WFR memory.

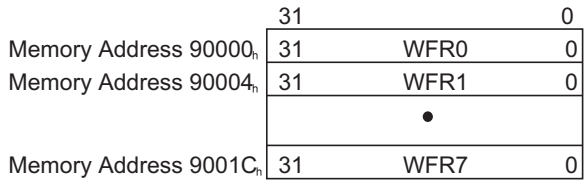


Figure B-4 WFR Memory Addressing

Table B-41 lists the bit definitions of the WFR registers.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU																											CB	Bit Count			

Table B-42 WFR Bit Definitions

Field/Bit Definition:

Bit Count — The number of bits in the waveform (4 to 12).

CB — If the dynamic clock is enabled (CLKCTRL bit 5) and data is set to two clocks per bit (CLKCTRL bit 4) then this defines the number of clocks per waveform bit (0 = two, 1 = one).

Notes:

None

3.2.4 Replace/Standby Register (REPREG:98000_h)

The replace register contains data that can be substituted based on a programed bank address and the associated enable bit is true.

The standby register becomes active during standby operation (Bit slice has released both memory banks).

The bank compare address is described in section 1.1.4.33.1.4.3.

Table B-41 lists the bit definitions of the replace register.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Standby Register																Replace Register															
M1	M2	TYPE			INDEX			DATA								M1	M2	TYPE			INDEX			DATA							

Table B-41 Replace/Standby Register Bit Definitions

Field/Bit Definition:

DATA — Bank memory “DATA” field replacement.

INDEX — DFR index (Waveform, Gap or Pause type) or LUT number (DATA or PRBS type).

TYPE — Transmit type.

Bit 13	Bit 12	Bit 11	Type
0	0	0	Waveform
0	0	1	NU
0	1	0	Programmable Gap
0	1	1	Transmitter Gap (fixed/random)
1	0	0	Data
1	0	1	Data with parity appended
1	1	0	PRBS
1	1	1	PRBS with parity appended

M2 — “TxMARKER2” level. (1 = logic high, 0 = logic low).

M1 — “TxMARKER1” level. (1 = logic high, 0 = logic low).

Notes:

None

3.2.5 Control Registers (BFCTRL)

The control registers are a set of three registers used to program the output, clock and offset functions.

The control registers are stored in an array of 3 long words illustrated below.

	31 ... 0
Memory Address $A0000_h$	Output Control
Memory Address $A0004_h$	Clock Control
Memory Address $A0008_h$	Offset Control
Memory Address $A000C_h$	Syncpulse Control
Memory Address $A0010_h$	Signal Control 1
Memory Address $A0014_h$	Signal Control 2
Memory Address $A0018_h$	Test Control

Figure B-6 Control Register Address Mapping

3.2.5.1 Output Control Register (OCTRL:$A0000_h$)

The output control register is used to program the enable bits of the data formatter.
Table B-43 list the bit definitions of the enable control register.

Bit #																											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	P	LBC		NU		BC		NU		M2C		NU		M1C		NU		SPC		NU		RSC		COC		SC		S1EN	S2EN	DC	

Table B-43 Output Control Register Bit Definition

Field/Bit Definition:

DC	Data Control, see note 1.
S1EN	Signal one enable (0 = Hi-Z, 1 = Data Format Controlled)
S2EN	Signal one enable (0 = Hi-Z, 1 = Data Format Controlled)
SC	Strobe Control, see note 1.
COC	Clock Output Control, see note 1.
RSC	Reference Select Control, see note 2.
SPC	Sync Pulse Control, see note 1.
M1C	Marker 1 Control, see note 1.
M2C	Marker 2 Control, see note 1.
BC	Busy Control, see note 1.
LBC	Last Bit Control, see note 1.
P	Compliment parity (1 = compliment, 0 = Don't compliment)

Notes:

1. The signal control is programmed according to the following table:

Bit 1	Bit 0	Signal Control
0	0	Force low.
0	1	Bit formatter output.
1	0	Force high.
1	1	Complimented bit formatter output.

2. The signal control is programmed according to the following table:

Bit 1	Bit 0	Signal Control
0	0	REFA
0	1	Bit formatter output.
1	0	REFB
1	1	Complimented bit formatter output.

3.2.5.2 Clock Control Register (CLKCTRL:$A0004_h$)

The clock control register allows the user to program the transmitter clock settings, divide value and clocks per bit selection.

Table B-45 list the bit definitions of the clock control register.

Bit #																												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU																					RXCO	COCS		ENRC	IC	EDC	CPB	DIV		DFCS	

Table B-45 Clock Control Register Bit Definition

Field/Bit Definition:

DFCS — Data Formatter Clock select

Bit 1	Bit 0	Clock
0	0	Internal Clock Generator
0	1	Front Panel TxClkIn
1	0	SYSCLK
1	1	VXI CLK10

DIV — Internal clock post divide.

Bit 3	Bit 2	Divide
0	0	1
0	1	10
1	0	100
1	1	1000

CPB — Clocks per bit (1 = One clock/bit, 0 = 2 clocks/bit).
EDC — Enable dynamic clock mode for waveforms (1 = enabled, 0 = disabled).
IC — Invert TxClkIn signal (1 = invert, 0 = normal).
ENRC — Enable TxClkIn as the reference clock for the internal clock generator, see note 1 (1 = enabled, 0 = disabled).
COCS — TxClkOut clock select

Bit 1	Bit 0	Clock
0	0	Internal Clock Generator
0	1	Front Panel TxClkIn
1	0	SYSCLK
1	1	VXI CLK10

RXCO — Clock output to Rx pair enable (1 = enabled, 0 = disabled).

Notes:

1. Refer to the XREF field of the clock generator register 3, section 3.2.10.3.

3.2.5.3 Offset Control Register (OFFCTRL:A0008$_h$)

This register contains the offset values for the marker outputs and reference selects.
Table B-44 list the bit definitions of the offset register:

Bit #																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X								BUSY-TE				BUSY-LE				MRK2-TE				MRK2-LE				MRK1-TE				MRK1-LE			

Table B-44 Offset Control Register Bit Description

Field/Bit Definition:

MRK1-LE — Marker 1 leading edge delay. (valid choices = 0x0-0xF).
MRK1-TE — Marker 1 trailing edge delay. (valid choices = 0x0-0xF).
MRK2-LE — Marker 2 leading edge delay. (valid choices = 0x0-0xF).
MRK2-TE — Marker 2 trailing edge delay. (valid choices = 0x0-0xF).
BUSY-LE — Busy leading edge delay. (valid choices = 0x0-0xF).
BUSY-TE — Busy trailing edge delay. (valid choices = 0x0-0xF).

Notes:

1. 0 = -6 clk delay, 6 = no delay, 0xF = 9 clk delay.

3.2.5.4 Syncpulse Control (SPCTRL:A000C$_h$)

This register contains the control bits for the syncpulse output.

Table B-51 list the bit definitions of the sync pulse control register:

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU								CD	CDE	CS	CRS	SPW				SPB															

Table B-46 Syncpulse Control Register Bit Description

Field/Bit Definition:

SPB	Sync Pulse Bit (Valid values: 0 = bit 1 to 65535 = bit 65536)
SPW	Sync Pulse Width (Valid values: 0 = 1 bit to 15 = 16 bits)
CRS	Compliment reference select during syncpulse (1 = compliment, 0 = don't).
CS	Compliment strobe during syncpulse (1 = compliment, 0 = don't).
CDE	Compliment data enable during syncpulse (1 = compliment, 0 = don't).
CD	Compliment data during syncpulse (1 = compliment, 0 = don't).

Notes:

None

3.2.5.5 Signal Control 1 (SIGCTRL1:A0010$_h$)

This register contains the control bits for the output signals.

Table B-47 list the bit definitions of signal control register one:

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIG8				SIG7				SIG6				SIG5				SIG4				SIG3				SIG2				SIG1			

Table B-47 Signal Control Register One Bit Definition

Field/Bit Definition:

SIG1	Signal 1 source, see notes below.
SIG2	Signal 2 source, see notes below.
SIG3	Signal 3 source, see notes below.
SIG4	Signal 4 source, see notes below.
SIG5	Signal 5 source, see notes below.
SIG6	Signal 6 source, see notes below.
SIG7	Signal 7 source, see notes below.
SIG8	Signal 8 source, see notes below.

Notes:

The signal source bits are programed according to the following table:

LSB + 3	LSB + 2	LSB + 1	LSB	Signal
0	0	0	0	DATA
0	0	0	1	CLKOUT
0	0	1	0	STROBE
0	0	1	1	MARKER1
0	1	0	0	MARKER2
0	1	0	1	FLAGOUT1
0	1	1	0	FLAGOUT2
0	1	1	1	BUSY

1	0	0	0	SYNCPULSE
1	0	0	1	Reserved
1	0	1	0	LASTBIT

3.2.5.6 Signal Control 2 (SIGCTRL2:A0014$_h$)

This register contains the control bits for the output signals.

Table B-51 list the bit definitions of the sync pulse control register:

Bit #																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU	IRSZ	DMODE		NU		I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	NU								SIG10				SIG9			

Table B-48 Signal Control Register 2 Bit Definition

Field/Bit Definition:

SIG9 Signal 9 source, see notes below.

SIG10 Signal 10 source, see notes below.

I1 - I10 Invert signal bits (I1 = SIG1, I2 = SIG2, etc.). 0 = non inverted, 1 = inverted.

DMODE Signal 1 and Signal 2 Data mode.

Bit 29	Bit 28	DEN	RSEL	Signal 1	Signal 2	Description
0	0	0	X	HI-Z	HI-Z	Bipolar/Differential with Tri-state and error
		1	0	S1DATA (VOHA, VOLA)	S2DATA (VOHA, VOLA)	
		1	1	S1DATA (VOHB, VOLB)	S2DATA (VOHB, VOLB)	
0	1	0	0	VOZ (VOLB)	VOZ (VOLB)	Bipolar/Differential with third state
		0	1	VOZ (VOHB)	VOZ (VOHB)	
		1	X	S1DATA (VOLA,VOHA)	S2DATA (VOLA,VOHA)	
1	0	0	0	VOZ (VOLB)	HI-Z	Bipolar with third state and error
		0	1	VOZ (VOHB)	HI-Z	
		1	0	S1DATA (VOHA, VOLA)	S2DATA (VOHA, VOLA)	
		1	1	S1DATA (VOHB, VOLB)	S2DATA (VOHA, VOLA)	

IRSZ Invert Reference Select VOZ data (1 = invert, 0 = normal).

Notes:

The signal source bits are programed according to the following table:

LSB + 3	LSB + 2	LSB + 1	LSB	Signal
0	0	0	0	DATA
0	0	0	1	CLKOUT
0	0	1	0	STROBE
0	0	1	1	MARKER1
0	1	0	0	MARKER2
0	1	0	1	FLAGOUT1
0	1	1	0	FLAGOUT2
0	1	1	1	BUSY
1	0	0	0	SYNCPULSE
1	0	0	1	Reserved
1	0	1	0	LASTBIT

3.2.5.7 Test Control Register (TESTCTRL:A0018$_h$)

This register contains the output selector and enable values for the test signals.

Table B-51 list the bit definitions of the test control register:

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU																												EN	SEL		

Table B-51 Test Control Register Bit Definition

Field/Bit Definition:

SEL Select the signal to test.

Bit 2	Bit 1	Bit 0	Test Signal
0	0	0	DATA
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

EN Enable the test signal (1 = enabled, 0 = disabled)

Notes:

None

3.2.6 Fixed/Random Delay Registers (DLYREG)

The Fixed/Random delay registers allow the user to program delays between data packets.

3.2.6.1 Fixed/Random Delay Register (MINMAX:A8000$_h$)

The random delay register allows the user to define a minimum and maximum random delay range.
Table B-49 list the bit definitions of the fixed delay register.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX																MIN															

Table B-49 Random Delay Register Bit Definition

Field/Bit Definition:

MIN Minimum delay value (0 = 4 clocks, FFFF$_h$ = 65539)
MAX Maximum delay value (0 = 4 clocks, FFFF$_h$ = 65539)

Notes:

None

3.2.6.2 Delay Status Register (DLYSTAT:A8004$_h$)

The delay readback register allows the user to query the current delay value.
Table B-50 list the bit definitions of the fixed delay register.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DLYMSB												NU																			

Table B-50 Fixed Delay Register Bit Definition

Field/Bit Definition:

DLYMSB Current delay value (upper 12 bits), read only.

Notes:

None

3.2.7 PRBS Seed (PRNSEED:B0000$_h$)

The PRN (pseudo random number) seed is used to initialize the random number generator.
This must be a non-zero number.

3.2.8 Run Control (TRUNREG:B8000$_h$)

The run control register allows the user to control the data formatter.
Table B-50 list the bit definitions of the run control register.

Bit #																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU																												RSP	FS0	RDELY	START

Table B-52 Run Control Bit Definition

Field/Bit Definition:

START	Start data formatter (1 = start pulse generated, 0 = no pulse)
RDELY	Reset delay function (1 = reset pulse generated, 0 = no pulse)
FS0	Force data format zero (1 = format zero enabled, 0 = normal operation)
RSP	Reset syncpulse counter (1 = reset, 0 = no pulse)

Notes:

None

3.2.9 Look Up Table Memory (DATA LUT:C0000$_h$)

The DATA LUT registers are segmented into eight pages of 256 words. Each page is selected by the "LUT" field from the bank memory or replace register.
The specific LUT page is then indexed by the "DATA" field from the bank memory or replace register.
Table B-53 lists the bit description of the DATA LUT memory.

Bit #																			
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DFRI				SCNT				RDATA											

Table B-53 DATA LUT Memory Definition

Field/Bit Definition:

RDATA	Replace Output data to send.
SCNT	Shift count for bits in the replaced data to send. (Min = 4, max = 12)
DFRI	Data format register index.

Notes:

None

3.2.10 Clock Generator Registers (TCLKGEN)

The clock generator registers allow the user to program the frequency of the internal clock generator.

Figure B-7 illustrates the four clock generator registers.

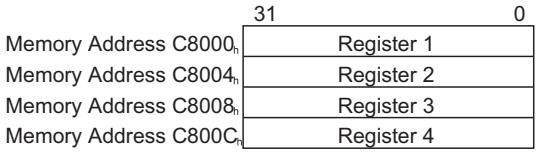


Figure B-7 Clock Generation Registers

The following sections describes the contents of the clock generator registers.

3.2.10.1 Clock Generator Register 1 (REG1:C8000$_h$)

Register 1 is initialized on power up to hex F00B0F0 and should not be modified.

3.2.10.2 Clock Generator Register 2 (REG2:C8004$_h$)

Register 2 programs the reference clock selection, post divide value and the lower 8 bits of the feedback divide value.

Table B-54 lists the bit description of the clock generator register 2.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEEDBACK 7:0								0	0	0	0	PD1		PD0		0	0	PD	RS	0	0	1	1	1	1	1	0	1	0	0	0

Table B-54 Clock Generator Register 2 Bit Definition

Field/Bit Definition:

RS — Reference Select (1 = external, 0 = internal)

PD — Power down (1 = power down, 0 = normal)

PD0 — Post Divide Zero

Bit 17	Bit 16	Divide
0	0	1
0	1	2
1	0	4
1	1	8

PD1 — Post Divide One

Bit 19	Bit 18	Divide
0	0	1
1	0	5

FEEDBACK 7:0 — Lower eight bits of the feedback divide value.

Notes:

None

3.2.10.3 Clock Generator Register 3 (REG3:C8008$_h$)

Register 3 programs the upper 6 bits of the feedback divide value, reference clock selection and the course tune value.

Table B-55 lists the bit description of the clock generator register 3.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	CTUNE				0	0	0	0	XREF			0	0	0	1	0	0	1	0	0	1	0	FEEDBACK 13:8					

Table B-55 Clock Generator Register 3 Bit Definition

Field/Bit Definition:

FEEDBACK 13:8	upper six bits of the feedback divide value.
XREF	External reference setting (0 = internal, 7 = external)
CTUNE	Course tune.

Notes:

None

3.2.10.4 Clock Generator Register 4 (REG4:C800C$_h$)

Register 4 is a write only register decode that starts the parallel to serial download into the chip.

3.2.11 Transmit Delay Control Register (TDCREG)

The output delay control registers allow the user to program the data formatter signal delays. Figure B-8 illustrates the output delay control registers.

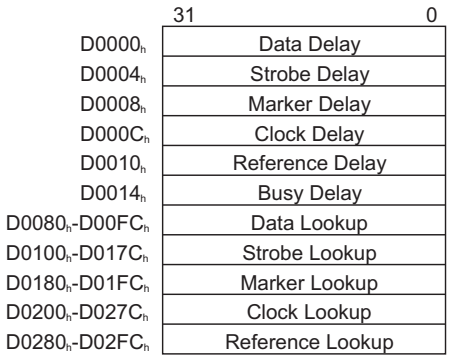


Figure B-8 Output Delay Control Memory

The following sections describes the contents of the output delay registers.

3.2.11.1 Data Delay Registers (DATA:D0000$_h$)

The data delay registers allow the user to program a delay value for TxDATA and its driver enable signal. Table B-56 lists the bit description of the data delay register.

Bit #																												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S2	LDENABLE					RDENABLE										S1	LDATA					RDATA									

Table B-56 Data Delay Register Bit Definition

Field/Bit Definition:

RDATA	Raw Data Delay Value (S = 0)
LDATA	Lookup Data Delay Address (S = 1)
S1	Select (0 = Raw value, 1 = Lookup value)
RDENABLE	Raw Data Enable Delay Value (S = 0)
LDENABLE	Lookup Data Enable Delay Address (S = 1)
S2	Select (0 = Raw value, 1 = Lookup value)

Notes:

None

3.2.11.2 Strobe Delay Registers (STROBE:D0004$_h$)

The strobe delay registers allow the user to program a delay value for TxSTROBE and its driver enable signal.

Table B-58 lists the bit description of the strobe delay register.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S2	LSPULSE					RSPULSE										S1	LSTROBE					RSTROBE									

Table B-58 Strobe Delay Register Bit Definition

Field/Bit Definition:

RSTROBE	Raw Strobe Delay Value (S = 0)
LSTROBE	Lookup Strobe Delay Address (S = 1)
S1	Select (0 = Raw value, 1 = Lookup value)
RSPULSE	Raw Syncpulse Delay Value (S = 0)
LSPULSE	Lookup Syncpulse Delay Address (S = 1)
S2	Select (0 = Raw value, 1 = Lookup value)

Notes:

None

3.2.11.3 Marker Delay Registers (MARKER:D0008$_h$)

The marker delay registers allow the user to program a delay value for TxMARKER1 and TXMARKER2.

Table B-57 lists the bit description of the marker delay register.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S2	LMKR2					RMKR2										S1	LMKR1					RMKR1									

Table B-57 Marker Delay Register Bit Definition

Field/Bit Definition:

RMKR1	Raw Marker1 Delay Value (S = 0)
LMKR1	Lookup Marker1 Delay Address (S = 1)
S1	Select (0 = Raw value, 1 = Lookup value)
RMKR2	Raw Marker2 Delay Value (S = 0)
LMKR2	Lookup Marker2 Delay Address (S = 1)
S2	Select (0 = Raw value, 1 = Lookup value)

Notes:

None

3.2.11.4 Clock Delay Registers (CLOCK:D000C$_h$)

The clock delay registers allow the user to program a delay value for TxCLKOUT and the selected data formatter clock.

Table B-59 lists the bit description of the clock delay register.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S2	LCLKOUT					RCLKOUT										S1	LCLKIN					RCLKIN									

Table B-59 Clock Delay Register Bit Definition

Field/Bit Definition:

RCLKIN	Raw Clock Input Delay Value (S = 0)
LCLKIN	Lookup Clock Input Delay Address (S = 1)
S1	Select (0 = Raw value, 1 = Lookup value)
RCLKOUT	Raw CLKOUT Delay Value (S = 0)
LCLKOUT	Lookup CLKOUT Delay Address (S = 1)

S2 Select (0 = Raw value, 1 = Lookup value)

Notes:

None

3.2.11.5 Reference Select Delay Registers (RSEL:D0010$_h$)

The reference delay registers allow the user to program a delay value for the reference select signal.

Table B-60 lists the bit description of the reference select delay register.

Bit #																												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S1	LRSEL					RRSEL										NU						CLKOUTAD									

Table B-60 Reference Select Delay Register Bit Definition

Field/Bit Definition:

CLKOUTAD CLKOUT alignment delay
RRSEL Raw Reference Select Delay Value (S = 0)
LRSEL Lookup Reference Select Delay Address (S = 1)
S1 Select (0 = Raw value, 1 = Lookup value)

Notes:

None

3.2.11.6 Busy Delay Registers (BUSYDLY:D0014$_h$)

The busy delay registers allow the user to program a delay value for the busy and last bit signals.

Table B-60 lists the bit description of the busy delay register.

Bit #																												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU						LBAD										NU						BUSYAD									

Table B-61 Busy Delay Adjust Register Bit Definition

Field/Bit Definition:

BUSYDA TxBUSY alignment delay
LBAD TxLastBit alignment delay

Notes:

1. Both delays are set to F9$_h$ on power up (15ns delay).

3.2.11.7 Data Delay Lookup Registers (DATALU:D0080$_h$-D00FC$_h$)

The data delay lookup registers allow the user to select a preprogrammed delay value for TxDATA and its driver enable signal.

The 32 registers are preprogrammed for delays from -15ns (offset 0) to +15ns (offset 78$_h$).

Table B-62 lists the bit description of the data delay lookup registers.

Bit #																												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU						LDENABLE										NU						LDATA									

Table B-62 Data Delay Lookup Register Bit Definition

Field/Bit Definition:

LDATA	Lookup Data Delay Value
LMCLK	Lookup Data Enable Delay Value

Notes:

None

3.2.11.8 Strobe Delay Lookup Registers (STROBELU:D0100$_h$-D017C$_h$)

The strobe delay registers allow the user to select a preprogrammed delay value for TxSTROBE and its driver enable signal.

The 32 registers are preprogrammed for delays from -15ns (offset 0) to +15ns (offset 78$_h$).

Table B-63 lists the bit description of the strobe delay lookup registers.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU						LSPULSE										NU						LSTROBE									

Table B-63 Strobe Delay Lookup Register Bit Definition

Field/Bit Definition:

LSTROBE	Lookup Strobe Delay Value
LSPULSE	Lookup Syncpulse Enable Delay Value

Notes:

None

3.2.11.9 Marker Delay Lookup Registers (MARKERLU:D0180$_h$-D01FC$_h$)

The marker delay registers allow the user to select a preprogrammed delay value for TxMARKER1 and TXMARKER2.

The 32 registers are preprogrammed for delays from -15ns (offset 0) to +15ns (offset 78$_h$).

Table B-64 lists the bit description of the marker delay lookup register.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU						LMKR2										NU						LMKR1									

Table B-64 Marker Delay Lookup Register Bit Definition

Field/Bit Definition:

LMKR1	Lookup Marker1 Delay Value
LMKR2	Lookup Marker2 Delay Value

Notes:

None

3.2.11.10 Clock Delay Lookup Registers (CLOCKLU:D0200$_h$-D027C$_h$)

The clock delay registers allow the user to select a preprogrammed delay value for TxCLKOUT and the selected data formatter clock.

The 32 registers are preprogrammed for delays from -15ns (offset 0) to +15ns (offset 78$_h$).

Table B-67 lists the bit description of the clock delay lookup registers.

Bit #																											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU						LCLKOUT										NU						LCLKIN									

Table B-67 Clock Delay Lookup Register Bit Definition

Field/Bit Definition:

LCLKIN Lookup CLKIN Delay Value
LCLKOUT Lookup CLKOUT Delay Value

Notes:

None

3.2.11.11 Reference Delay Lookup Registers (RSELLU:D0280$_h$-D02FC$_h$)

The reference delay registers allow the user to select a preprogrammed delay value for the reference select signal.

The 32 registers are preprogrammed for delays from -15ns (offset 0) to +15ns (offset 78$_h$).

Table B-65 lists the bit description of the reference select delay lookup registers.

Bit #																											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU						LRSEL										NU															

Table B-65 Data Delay Lookup Register Bit Definition

Field/Bit Definition:

LRSEL Lookup Reference Select Delay Value

Notes:

None

3.2.12 Data Formatter Interrupt Control Registers (DFINTR)

The interrupt control registers allow the user to map and enable interrupt generation.

The control registers are mapped as described below.

Address LSB			Name	Offset	Description
A4	A3	A2			
0	0	0	DFPTE	F0000h	Positive Transition Enable
0	0	1	DFNTE	F0004h	Negative Transition Enable
0	1	0	DFIRQEN	F0008h	Interrupt Enable
0	1	1	DFINT	F000Ch	Interrupt Register
1	0	0	DFEVENT	F0010h	Event Register

Table B-66 Interrupt Control Registers

3.2.12.1 Data Formatter Positive Transition Enable (DFPTE:F0000$_h$)

This register allows the user to program the event mask register for events going positive.

Table B-69 lists the bit description of the positive transition enable register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU		SCERR	PRBS	DATA	TGAP	PGAP	WF	M2	M1	SPC	RDC	MEM	BUSY	STBY	NOCLK

Table B-69 Data Formatter Positive Transition Enable Bit Definition

Field/Bit Definition:

NOCLK	No Clock; Slow or missing data formatter clock (1 = no clock).
STBY	Standby active (0 = active).
BUSY	Transmit active (1 = active).
MEM	Memory active (0 = A, 1 = B).
RDC	Replace Data Compare (1 = compare true).
SPC	Sync Pulse Compare (1 = compare true).
M1	Marker one level (0 = low, 1 = high).
M2	Marker two level (0 = low, 1 = high).
WF	Waveform active (1 = active).
PGAP	Programmable gap active (1 = active).
TGAP	Transmitter gap active (1 = active).
DATA	Data active (1 = active).
PRBS	PRBS active (1 = active).
SCERR	Shift count error (1 = error).

Notes:

1. 0 = disable positive event transition, 1 = enable event on low to high transition.

3.2.12.2 Data Formatter Negative Transition Enable (DFNTE:F0004$_h$)

This register allows the user to program the event mask register for events going negative.

Table B-68 lists the bit description of the negative transition enable register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU		SCERR	PRBS	DATA	TGAP	PGAP	WF	M2	M1	SPC	RDC	MEM	BUSY	STBY	NOCLK

Table B-68 Data Formatter Negative Transition Enable

Field/Bit Definition:

NOCLK	No Clock; Slow or missing data formatter clock (1 = no clock).
STBY	Standby active (0 = active).
BUSY	Transmit active (1 = active).
MEM	Memory active (0 = A, 1 = B).
RDC	Replace Data Compare (1 = compare true).
SPC	Sync Pulse Compare (1 = compare true).
M1	Marker one level (0 = low, 1 = high).
M2	Marker two level (0 = low, 1 = high).
WF	Waveform active (1 = active).
PGAP	Programmable gap active (1 = active).
TGAP	Transmitter gap active (1 = active).
DATA	Data active (1 = active).
PRBS	PRBS active (1 = active).
SCERR	Shift count error (1 = error).

Notes:

1. 0 = disable negative event transition, 1 = enable event on high to low transition

3.2.12.3 Data Formatter Interrupt Event Enable Register (DFIRQEN:F0008$_h$)

This register allows the user to program specific event to cause an interrupt.

Table B-70 lists the bit description of the event enable register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU		SCERR	PRBS	DATA	TGAP	PGAP	WF	M2	M1	SPC	RDC	MEM	BUSY	STBY	NOCLK

Table B-70 Data Formatter Interrupt Event Enable Register Bit Definition

Field/Bit Definition:

NOCLK	No Clock; Slow or missing data formatter clock (1 = no clock).
STBY	Standby active (0 = active).
BUSY	Transmit active (1 = active).
MEM	Memory active (0 = A, 1 = B).
RDC	Replace Data Compare (1 = compare true).
SPC	Sync Pulse Compare (1 = compare true).
M1	Marker one level (0 = low, 1 = high).
M2	Marker two level (0 = low, 1 = high).
WF	Waveform active (1 = active).
PGAP	Programmable gap active (1 = active).
TGAP	Transmitter gap active (1 = active).
DATA	Data active (1 = active).
PRBS	PRBS active (1 = active).
SCERR	Shift count error (1 = error).

Notes:

1. 0 = disable event interrupt, 1 = enable event interrupt

3.2.12.4 Interrupt Register (DFINT:F000C$_h$)

This register allows the user to query the current status of the interrupt bits.

Table B-71 lists the bit description of the event enable register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU		SCERR	PRBS	DATA	TGAP	PGAP	WF	M2	M1	SPC	RDC	MEM	BUSY	STBY	NOCLK

Table B-71 Data Formatter Interrupt Register Bit Definitions

Field/Bit Definition:

NOCLK	No Clock; Slow or missing data formatter clock (1 = no clock).
STBY	Standby active (0 = active).
BUSY	Transmit active (1 = active).
MEM	Memory active (0 = A, 1 = B).
RDC	Replace Data Compare (1 = compare true).
SPC	Sync Pulse Compare (1 = compare true).
M1	Marker one level (0 = low, 1 = high).
M2	Marker two level (0 = low, 1 = high).
WF	Waveform active (1 = active).
PGAP	Programmable gap active (1 = active).
TGAP	Transmitter gap active (1 = active).
DATA	Data active (1 = active).
PRBS	PRBS active (1 = active).
SCERR	Shift count error (1 = error).

Notes:

None

3.2.12.5 Data Formatter Interrupt Event Register (DFEVENT:F0010$_h$)

This register allows the user to query the interrupt event status. This register is cleared after it is queried.
Table B-72 lists the bit description of the interrupt event register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU		SCERR	PRBS	DATA	TGAP	PGAP	WF	M2	M1	SPC	RDC	MEM	BUSY	STBY	NOCLK

Table B-72 Data Formatter Interrupt Event Register Bit Definition

Field/Bit Definition:

NOCLK	No Clock; Slow or missing data formatter clock (1 = no clock).
STBY	Standby active (0 = active).
BUSY	Transmit active (1 = active).
MEM	Memory active (0 = A, 1 = B).
RDC	Replace Data Compare (1 = compare true).
SPC	Sync Pulse Compare (1 = compare true).
M1	Marker one level (0 = low, 1 = high).
M2	Marker two level (0 = low, 1 = high).
WF	Waveform active (1 = active).
PGAP	Programmable gap active (1 = active).
TGAP	Transmitter gap active (1 = active).
DATA	Data active (1 = active).
PRBS	PRBS active (1 = active).
SCERR	Shift count error (1 = error).

Notes:

1. 1 = event true, 0 = event false.

3.2.13 Data Formatter Revision/Status Register (DFREV:F8000$_h$)

The revision register contains the Data Formatter revision/status code.
Table B-73 lists the bit description of the data formatter/status register.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X															CA	DFVER								DFREV							

Table B-73 Data Formatter/Status Bit Definition

Field/Bit Definition:

DFREV	Data Formatter Revision.
DFVER	Data Formatter Version.
CA	Clock Active (1 = Clock < 500Hz)

Notes:

None

3.3 Transmitter CMT Memory (CMTDATA:200000$_h$)

The CMT (Command Memory Table) memory is segmented into two banks (A and B) each containing 512K command words.

The CMT bank memory addressing is illustrated below.

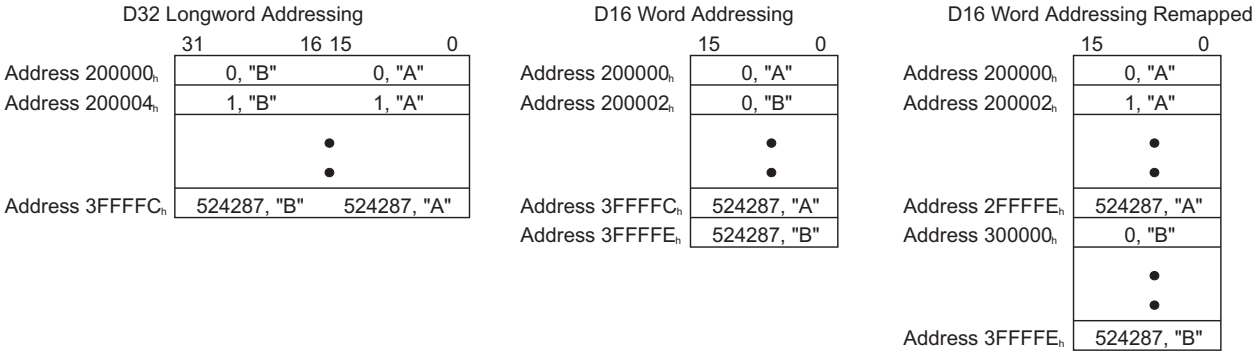


Figure B-9 CMT Memory Addressing

Each command word contains a data field and a command field described below.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Command								Data							
M1	M2	TYPE			INDEX			DINDEX							

Table B-74 CMT Memory Bit Definition

Field Bit Definition:

DINDEX Data index into the selected LUT (0 - 255).
INDEX Selects either the LUT or WFR based on “TYPE” (0 - 7)
TYPE Data type.

Bit 13	Bit 12	Bit 11	Data Type
0	0	0	Output Waveform.
0	0	1	Reserved.
0	1	0	Output Programmable Intermessage Gap.
0	1	1	Output Transmitter Gap (Fixed/Random).
1	0	0	Output LUT data.
1	0	1	Output LUT data with parity appended.
1	1	0	Output PRBS data.
1	1	1	Output PRBS data with parity appended.

M2 TxMARKER2 level (0 = low, 1 = high).
M1 TxMARKER1 level (0 = low, 1 = high).

Notes:

1. Access to the CMT memory is controlled through the MEMCTRL register, see section 3.1.4.7.

4 2108Rx Register Map

The 2108Rx device is segmented in to three major segments. Table B-75 below lists the address map of the Talon 2108Rx major segments.

Major Segment Code			Major Segment Name	Base Address Range	Description
A21	A20	A19			
0	0	X	RXREG	0h	Receiver Registers.
0	1	0	IFCREG	100000h	Interface Registers.
1	X	X	BANKAB	200000h	Bank A and B Memory 32 Bit Access.

Table B-75 Model 2108 Receiver Address Bit Definition

4.1 Receiver Register Description (RXREG)

The receiver registers segments are described below:

Register Segment Code (RSC)				Register Segment Name	Base Address RXMEM + RSC	Description
A18	A17	A16	A15			
0	0	0	0	RVXIREG	0h	Receiver VXI Register Memory
0	0	0	1	TRIG	8000h	Trigger Memory
0	0	1	0	QUAL	10000h	Qualifier Memory
0	0	1	1	TCMD	18000h	Trigger Command Memory
0	1	0	0	RCONTROL	20000h	Receiver Control Registers
0	1	0	1	RDELAY	28000h	Receiver Delay Control Registers
0	1	1	0	RCLKGEN	30000h	Receiver Clock Generator Registers
0	1	1	1	RRUN	38000h	Receiver Run Control Registers
1	1	1	0	RINTR	70000h	Interrupt Control Registers
1	1	1	1	RREV	78000h	Receiver Revision

Table B-77 Receiver Register Segment List

The following sections describes the registers of the 2108 Receiver memory.

4.1.1 Receiver VXI Register Memory (RVXIREG,R:0_h)

This register contains the VXI A16 ID and DEVICE register data for the 2108 receiver module.
Table B-76 lists the bit definitions of the VXI register.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Device Type																ID															

Table B-76 Receiver VXI Register Bit Definition

Field Bit Definition:

ID — VXI ID register. ($DF0F_h$)
Device Type — VXI Device Type Register. (9120_h)

Notes:

None

4.1.2 Trigger Memory (TRIG,R/W:8000_h)

This memory contains the trigger patterns for the 2108 receiver module. The trigger memory can be configured as either sixteen 32 bit trigger patterns or 8 64 bit trigger patterns.

The trigger pattern is stored in an array of 128 long words illustrated below.

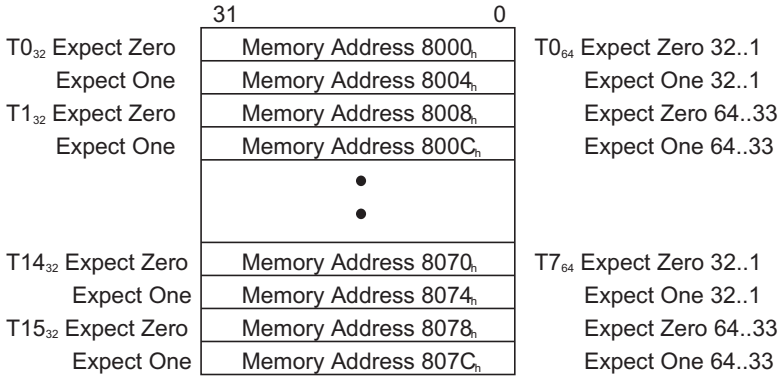


Figure B-11 Bit Slice Memory Addressing

Table B-8 lists the bit definitions of the trigger pattern memory.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Input data is compared starting with bit 0, i.e., bit 31 is the oldest sample bit, bit 0 is the current sample bit																													

Table B-78 Trigger Pattern Bit Definition

Field/Bit Definition:

Bit 0-31 Expect one/zero pattern compared to the input data.

Expect One	Expect Zero	Input Compare
0	0	Expect middle state, i.e., not good1 or good0.
0	1	Expect a good 0.
1	0	Expect a good 1.
1	1	Mask bit off.

Notes:

1. In the 64 bit trigger mode the odd trigger is appended to the even trigger number, e.g., T0$_{32}$ and T1$_{32}$ becomes T0$_{64}$. The odd trigger number stores the expect data for bits 33 to 64 and the even trigger number stores the expect data for bits 1 through 32.

4.1.3 Qualifier Memory (QUAL,R/W:10000$_h$)

This memory contains the expect and mask codes for the front panel RxQUAL1/2 signals. Each of the sixteen triggers can specify a qualifier pattern.

The qualifier patterns are stored in four registers illustrated below:

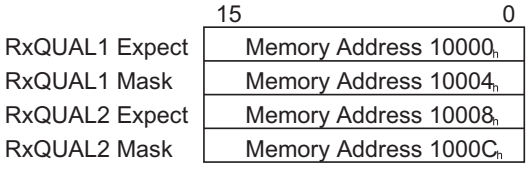


Figure B-10 Qualifier Memory Addressing

Table B-80 lists the bit definitions of the qualifier memory.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0

Table B-80 Qualifier Pattern Bit Definition

Field Bit Definition:

T0-T15 Expect and mask values for the corresponding trigger number.

Mask	Expect	Input Compare
0	0	Expect good0.
0	1	Expect good 1.
1	X	Mask qualifier off

Notes:

None

4.1.4 Trigger Command Memory (TCMD,R/W:18000_h)

The trigger command memory allows the user to program a trigger sequence.

There are sixteen command sequences, each command sequence can have up to sixteen trigger command. Each trigger command can enable any of the trigger patterns.

The trigger command memory addressing is illustrated below:

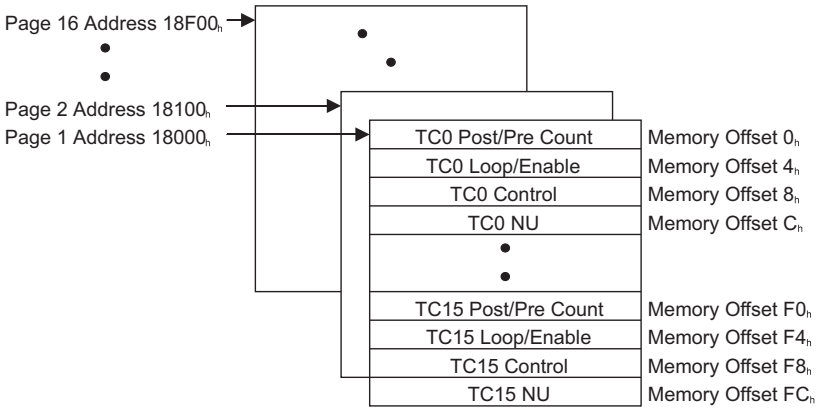


Figure B-12 Trigger Command Memory Addressing

Table B-79 lists the bit definitions of the trigger command memory “Post/Pre Count” registers.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Post Count																				Pre Count											

Table B-79 Trigger Command Post/Pre Register Bit Definition

Field Bit Definition:

Pre Count Number of eight bit words to record prior to the trigger.

Post Count Number of eight bit words to record after the trigger (0 = continuous).

Notes:

None

Table B-83 lists the bit definitions of the trigger command memory “Loop/Enable” registers.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Loop Count																Enable															

Table B-83 Trigger Command Loop/Enable Register Bit Definition

Field Bit Definition:

Enable	A one in any bit position enables the corresponding trigger pattern.
Loop Count	Number of loops for this trigger command. (0 to 65535, 0 = continuous).

Notes:

None

Table B-81 lists the bit definitions of the trigger command memory “Control” registers.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X																														W	LS

Table B-81 Trigger Command Control Register Bit Definition

Field Bit Definition:

LS	Last Sequence bit. (1 = last trigger command, 0 = not last).
W	Wait for transmitter acknowledge flag. (1 = wait, 0 = don’t wait).

Notes:

None

4.1.5 Receiver Control/Status Register (RCONTROL)

These three registers allow the user to control and query 2108 receiver functions.

The control/status register addressing is illustrated below.

General Control/Status	Memory Address 20000_h
Clock Control	Memory Address 20004_h
Memory Control	Memory Address 20008_h
Output Control	Memory Address $2000C_h$

Figure B-13 Receiver Status/Control Register Address Map

4.1.5.1 General Control/Status Register (ICTRL,R/W:20000_h)

This register one allows the user to query and control the receiver functions listed below.

Table B-82 lists the bit definitions of the control/status memory.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STOP	PREL	MERR	CERR	HFCRL	LFCRE	LFCRS	LFCRF	LCMD	WAIT	ARM	BUSY	CMD				NU		HFLSE	TASE	IMBEN	TAQ2	TAQ1	TMODE	PAGE				SCMD			

Table B-82 Input Register Bit Definition

Field Bit Definition:

SCMD	Start Command Number.
PAGE	Command Sequence Page Number.
TMODE	Trigger Mode (1 = 64 bit, 0 = 32 bit).

TAQ1	TxQUAL1 source, 0 = front panel, 1 = TRIGA
TAQ2	TxQUAL2 source, 0 = front panel, 1 = TRIGA
IMBEN	Inter Module Bus Enable. (1 = enable, 0 = not).
TASE	Input trigger (TRIGA) start enable, see note 2 (1 = enabled, 0 = disabled).
HFLSE	High frequency lock start enable, see note 2 (1 = enabled, 0 = disabled).
CMD	Current command number.
BUSY	Busy flag. (1 = Receiver busy)
ARM	Armed. (1 = receiver waiting for trigger pattern).
WAIT	Waiting for transmitter acknowledge. (1 = waiting).
LCMD	Last Command. (1 = last command of sequence).
LFCRF	Low Frequency Clock Recovery Fast flag. (1 = data rate too fast).
LFCRS	Low Frequency Clock Recovery Slow flag. (1 = data rate too slow).
LFCRE	Low Frequency Clock Recovery Error flag. (1 = data rate error).
HFCRL	High Frequency Clock Recovery Lock flag (1 = clock recovery Locked).
CERR	Clock Error (1 = Clock < ~480Hz).
MERR	Memory Error (1 = attempt to record when not released).
PREL	Preload flag (1 = memory preloading).
STOP	Stop flag (1 = force stop in progress).

Notes:

1. Bits 16 to 31 are read only.
2. A high to low transition start the receiver.

4.1.5.2 Clock Control Register (CLKCTRL,R/W:20004_h)

The clock control register allows the user to query and control the receiver clock settings listed below. Table B-82 lists the bit definitions of the clock control register.

Bit #																												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X																					FS			IC	DSEL		DIV		CSEL		

Table B-84 Clock Control Register Bit Definition

Field/Bit Definition:

CSEL — Clock Select

Bit 2	Bit 1	Bit 0	Clock
0	0	0	Internal Clock Generator
0	0	1	External Front Panel
0	1	0	SYSCLK
0	1	1	VXI CLK10
1	0	0	Low Frequency Recovered Clock
1	0	1	High Frequency Recovered Clock
1	1	0	Test Clock
1	1	1	SYSCLK

DIV — Internal Clock post divide.

Bit 4	Bit 3	Divide
0	0	1
0	1	10
1	0	100
1	1	1000

DSEL — Data Select

Bit 6	Bit 5	Data Source
0	0	Front Panel (RxDATA)
0	1	High Frequency Recovered data
1	0	Test Data
1	1	Receiver ClkIn

IC — Invert Receiver ClkIn signal (1 = invert, 0 = do not invert).

FS — Frequency Range Select (High Frequency Clock Recovery)

Bit 10	Bit 9	Bit 8	Clock Range MHz
0	0	0	32-52
0	0	1	47-78
0	1	0	63-104
0	1	1	94-157
1	0	0	125-208

Notes:

None.

4.1.5.3 Memory Control Register (RMEMCTRL,R/W:20008$_h$)

The memory control register allows the user to query and control the receiver clock settings listed below. Table B-87 lists the bit description of the good0/good1delay register.

Bit #																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU																										GRNTB	GRNTA	BSYB	BSYA	REQB	REQA

Table B-85 Memory Control Register Bit Definition

Field/Bit Definition:

REGA	Request Memory A. (1 = request, 0 = release)
REQB	Request Memory B. (1 = request, 0 = release).
BSYA	Memory A Busy. (1 = busy)
BSYB	Memory B Busy. (1 = busy)
GRNTA	Memory A Granted. (1 = memory A granted).
GRNTB	Memory B Granted. (1 = memory B granted).

Notes:

1. Bits two to five are read only.

4.1.5.4 Output Control Register (ROCTRL,R/W:2000C$_h$)

The output control register allows the user to set and query receiver output settings listed below. Table B-86 lists the bit description of the good0/good1delay register.

Bit #																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU																		TBEN	ENRC	GVS	ENGV	TNEN	TVEN	S2EN	S2SEL			S1EN	S1SEL		

Table B-86 Output Control Register Bit Definitions

Field/Bit Definition:

S1SEL	Signal one select bits (see note 1 below).
S1EN	Signal one enable (1 = enabled, 0 = disable).
S2SEL	Signal two select bits (see note 1 below).
S2EN	Signal two enable (1 = enabled, 0 = disable).
TVEN	Trigger valid enable (1 = enabled, 0 = disable).
TNEN	Trigger number enable (1 = enabled, 0 = disable).
ENGV	G1VAL, G0VAL and CLKOUT enable (1 = enabled, 0 = disable).
GVS	Good value select (1 = Qual1/Qual2, 0 = G0Val/G1Val).
ENRC	Reference clock enable (1 = enabled, 0 = disable).
TBEN	Output trigger (TRIGB) enable, source is TrigValid.

Notes:

1. The signal select codes are defined below:

Bit 2	Bit 1	Bit 0	Data Source	
			SIG1	SIG2
0	0	0	RxARM	
0	0	1	RxBUSY	
0	1	0	WAIT	TDIS
0	1	1	TxACK	
1	0	0	LOSTCLK	
1	0	1	HFCR-ERR	HFCR-ND
1	1	0	MEMABSY	MEMBBSY
1	1	1	LFCR-DEV	LFCR-ERR

RxARM Armed (1 = receiver waiting for trigger).
RxBUSY Busy (1 = receiver running).
WAIT Receiver wait signal from the command word used in the transmitter handshake mode (1 = wait for acknowledge).
TDIS Trigger disabled (post trigger recording or waiting for acknowledge from transmitter).
TxACK Acknowledge signal from transmitter.
LOSTCLK Clock error signal (1 = clock < ~480Hz).
HFCR-ERR High frequency clock recovery error (1 = lost lock).
HFCR-ND High frequency clock recovery no data (1 = not enough data transitions).
MEMABSY Memory bank “A” busy (1 = busy).
MEMBBSY Memory bank “B” busy (1 = busy).
LFCR-DEV Low frequency clock recovery deviation, clock frequency too fast or too slow (1 = clock adjustment recommended).
LFCR-ERR Low frequency clock recovery error (1 = error).

2. The training clock is used for the HFCR and should be disable when HFCR is not selected.
3. The reference clock is used to provide an external signal to the clock generator. Disable this signal when the internal clock reference is selected.

4.1.6 Receiver Delay Control Register (RDCREG:28000_h)

The receiver delay control registers allow the user to program the signal delays.

Figure B-14 illustrates the receiver delay control registers.

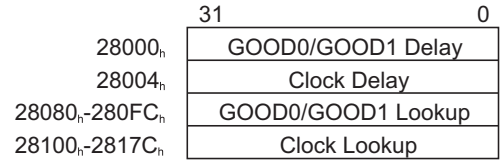


Figure B-14 ReceiverDelay Control Memory

The following sections describes the contents of the delay control registers.

4.1.6.1 GOOD0/GOOD1 Delay Registers (G0_G1:28000_h)

The good0/good1 delay registers allow the user to program a delay value for translated RxDATA signals.

Table B-87 lists the bit description of the good0/good1delay register.

Bit #																												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S2	LGOOD1					RGOOD1										S1	LGOOD0					RGOOD0									

Table B-87 Good0/Good1 Delay Register Bit Definition

Field/Bit Definition:

RGOOD0	Raw Good0 Delay Value (S = 0)
LGOOD0	Lookup Good0 Delay Address (S = 1)
S1	Select (0 = Raw value, 1 = Lookup value)
RGOOD1	Raw Good1 Delay Value (S = 0)
LGOOD1	Lookup Good1 Delay Address (S = 1)
S2	Select (0 = Raw value, 1 = Lookup value)

Notes:

None.

4.1.6.2 Clock Delay Registers (CLOCK:28004$_h$)

The clock delay registers allow the user to program a delay value for data clock signal.

Table B-88 lists the bit description of the clock delay register.

Bit #																												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S1	LCLOCK					RCLOCK										X															

Table B-88 Strobe Delay Register Bit Definition

Field/Bit Definition:

RCLOCK	Raw Clock Delay Value (S = 0)
LCLOCK	Lookup Clock Delay Address (S = 1)
S1	Select (0 = Raw value, 1 = Lookup value)

Notes:

None.

4.1.6.3 Good1/0 Delay Lookup Registers (G0_G1LU:28080$_h$-280FC$_h$)

The good1/0 delay lookup registers allow the user to select a preprogrammed delay value for good1 and good0 receiver signals.

The 32 registers are preprogrammed for delays from -15ns (offset 0) to +15ns (offset 78$_h$).

Table B-89 lists the bit description of the good1/0 delay lookup registers.

Bit #																												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X						LGOOD1										X						LGOOD0									

Table B-89 Good1/0 Delay Lookup Register Bit Definition

Field/Bit Definition:

LGOOD0	Lookup Data Delay Value
LGOOD1	Lookup Data Enable Delay Value

Notes:

None.

4.1.6.4 Clock Delay Lookup Registers (CLOCKLU:28100$_h$-2817C$_h$)

The clock delay registers allow the user to select a preprogrammed delay value for receiver clock signal.

The 32 registers are preprogrammed for delays from -15ns (offset 0) to +15ns (offset 78$_h$).

Table B-91 lists the bit description of the clock delay lookup registers.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X						LCLOCK										X															

Table B-91 Clock Delay Lookup Register Bit Definition

Field/Bit Definition:

LCLOCK Lookup Clock Delay Value

Notes:

None.

4.1.7 Clock Generator Registers (RCLKGEN)

The clock generator registers allow the user to program the frequency of the internal receiver clock generator.

Figure B-15 illustrates the four clock generator registers.

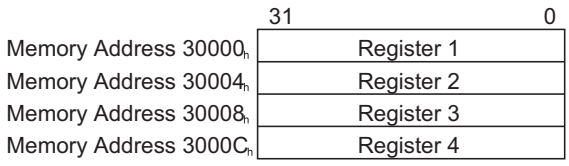


Figure B-15 Clock Generation Registers

The following sections describes the contents of the clock generator registers.

4.1.7.1 Clock Generator Register 1 (REG1:30000_h)

Register 1 is initialized on power up to hex F00B0F0 and should not be modified.

4.1.7.2 Clock Generator Register 2 (REG2:30004_h)

Register 2 programs the reference clock selection, post divide value and the lower 8 bits of the feedback divide value.

Table B-90 lists the bit description of the clock generator register 2.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEEDBACK 7:0								0	0	0	0	PD1		PD0		0	0	PD	RS	0	0	1	1	1	1	1	0	1	0	0	0

Table B-90 Clock Generator Register 2 Bit Definition

Field/Bit Definition:

RS Reference Select (1 = external, 0 = internal)
PD Power down (1 = power down, 0 = normal)
PD0 Post Divide Zero

Bit 17	Bit 16	Divide
0	0	1
0	1	2
1	0	4
1	1	8

PD1 Post Divide One

Bit 19	Bit 18	Divide
0	0	1
1	0	5

FEEDBACK 7:0 Lower eight bits of the feedback divide value.

Notes:

1. If ‘RS’ is set to internal(0) then the ‘ENRC’ bit of the output control register should be set to disabled(0).

4.1.7.3 Clock Generator Register 3 (REG3:30008$_h$)

Register 3 programs the upper 6 bits of the feedback divide value, reference clock selection and the course tune value.

Table B-92 lists the bit description of the clock generator register 3.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	CTUNE				0	0	0	0	XREF			0	0	0	1	0	0	1	0	0	1	0	FEEDBACK 13:8					

Table B-92 Clock Generator Register 3 Bit Definition

Field/Bit Definition:

FEEDBACK 13:8 upper six bits of the feedback divide value.
XREF External reference setting (0 = internal, 7 = external)
CTUNE Course tune.

Notes:

None.

4.1.7.4 Clock Generator Register 4 (REG4:3000C$_h$)

Register 4 is a write only register decode that starts the parallel to serial download into the chip.

4.1.8 Run Control Register (RRUNREG:38000$_h$)

The run control register allows the user to start/stop the 2108 receiver.

Table B-93 lists the bit description of the run control register.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU																										STOP	PRE	FIN	RUN	RST	CLR

Table B-93 2108RX Run Control Bit Definition

Field/Bit Definition:

CLR Clear the input pipeline.
RST Reset the command sequence.
RUN Begin data/trigger capture.
FIN Finish recording data in pipeline.
PRE Preload the record memory.
STOP Stop the receiver.

Notes:

1. All signal are written active high and are self resetting.

4.1.9 Receiver Interrupt Control Registers (RINTR)

The interrupt control registers allow the user to map and enable interrupt generation.
The control registers are mapped as described below.

Address LSB					Name	Size	Description
A4	A3	A2	A1	A0			
0	0	0	X	X	RPTE	70000h	Positive Transition Enable
0	0	1	X	X	RNTE	70004h	Negative Transition Enable
0	1	0	X	X	RIRQEN	70008h	Interrupt Enable
0	1	1	X	X	RINT	7000Ch	Interrupt Register
1	0	0	X	X	REVENT	70010h	Event Register

Table B-96 2108RX Interrupt Registers

4.1.9.1 Receiver Positive Transition Enable (RPTE:70000_h)

This register allows the user to program the event mask register for events going low to high.
Table B-94 lists the bit description of the positive transition enable register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TACK	TDIS	WAIT	BUSY	ARM	MEMB	MEMA	HFCRE	HFCRD	LFCRE	LFCRD	LFCRS	LFCRF	SE	MERR	NOCLK

Table B-94 Receiver Positive Transition Enable Bit Definition

Field/Bit Definition:

NOCLK	No Clock; Slow or missing clock.
MERR	Memory Error;
SE	Start Error;
LFCRF	Low Frequency Clock Recovery too Fast.
LFCRS	Low Frequency Clock Recovery too Slow.
LFCRD	Low Frequency Clock Recovery Deviation.
LFCRE	Low Frequency Clock Recovery Error.
HFCRD	High Frequency Clock Recovery No Data.
HFCRE	High Frequency Clock Recovery Error.
MEMA	Bank A memory busy.
MEMB	Bank B memory busy.
ARM	Receiver armed.
BUSY	Receiver busy
WAIT	Receiver Waiting
TDIS	Trigger Disabled.
TACK	TxAck Signal

Notes:

1. 0 = disable positive event transition, 1 = enable event on low to high transition.

4.1.9.2 Receiver Negative Transition Enable (RNTE:70004_h)

This register allows the user to program the event mask register for events going negative.
Table B-22 lists the bit description of the negative transition enable register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TACK	TDIS	WAIT	BUSY	ARM	MEMB	MEMA	HFCRE	HFCRD	LFCRE	LFCRD	LFCRS	LFCRF	SE	MERR	NOCLK

Table B-95 Receiver Negative Transition Enable

Field/Bit Definition:

NOCLK	No Clock; Slow or missing clock.
MERR	Memory Error;
SE	Start Error;
LFCRF	Low Frequency Clock Recovery too Fast.
LFCRS	Low Frequency Clock Recovery too Slow.
LFCRD	Low Frequency Clock Recovery too Deviation.
LFCRE	Low Frequency Clock Recovery too Error.
HFCRD	High Frequency Clock Recovery No Data.
HFCRE	High Frequency Clock Recovery Error.
MEMA	Bank A memory busy.
MEMB	Bank B memory busy.
ARM	Receiver armed.
BUSY	Receiver busy
WAIT	Receiver Waiting
TDIS	Trigger Disabled.
TACK	TxAck Signal

Notes:

1. 0 = disable negative event transition, 1 = enable event on high to low transition

4.1.9.3 Receiver Interrupt Event Enable Register (RIRQEN:70008_h)

This register allows the user to program specific event to cause an interrupt.

Table B-97 lists the bit description of the event enable register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TACK	TDIS	WAIT	BUSY	ARM	MEMB	MEMA	HFCRE	HFCRD	LFCRE	LFCRD	LFCRS	LFCRF	SE	MERR	NOCLK

Table B-97 Receiver Interrupt Event Enable Register Bit Definition

Field/Bit Definition:

NOCLK	No Clock; Slow or missing clock.
MERR	Memory Error;
SE	Start Error;
LFCRF	Low Frequency Clock Recovery too Fast.
LFCRS	Low Frequency Clock Recovery too Slow.
LFCRD	Low Frequency Clock Recovery too Deviation.
LFCRE	Low Frequency Clock Recovery too Error.
HFCRD	High Frequency Clock Recovery No Data.
HFCRE	High Frequency Clock Recovery Error.
MEMA	Bank A memory busy.
MEMB	Bank B memory busy.
ARM	Receiver armed.
BUSY	Receiver busy
WAIT	Receiver Waiting
TDIS	Trigger Disabled.
TACK	TxAck Signal

Notes:

1. 0 = disable event interrupt, 1 = enable event interrupt

4.1.9.4 Interrupt Register (RINT:$7000C_h$)

This register allows the user to query the current status of the interrupt bits.

Table B-99 lists the bit description of the event enable register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TACK	TDIS	WAIT	BUSY	ARM	MEMB	MEMA	HFCRE	HFCRD	LFCRE	LFCRD	LFCRS	LFCRF	SE	MERR	NOCLK

Table B-99 Interrupt Register Bit Definitions

Field/Bit Definition:

NOCLK	No Clock; Slow or missing clock.
MERR	Memory Error;
SE	Start Error;
LFCRF	Low Frequency Clock Recovery too Fast.
LFCRS	Low Frequency Clock Recovery too Slow.
LFCRD	Low Frequency Clock Recovery too Deviation.
LFCRE	Low Frequency Clock Recovery too Error.
HFCRD	High Frequency Clock Recovery No Data.
HFCRE	High Frequency Clock Recovery Error.
MEMA	Bank A memory busy.
MEMB	Bank B memory busy.
ARM	Receiver armed.
BUSY	Receiver busy.
WAIT	Receiver Waiting
TDIS	Trigger Disabled.
TACK	TxAck Signal.

Notes:

1. All signal are active high.

4.1.9.5 Receiver Interrupt Event Register (BSEVENT:70010_h)

This register allows the user to query the interrupt event status. This register is cleared after it is queried. Table B-98 lists the bit description of the interrupt event register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TACK	TDIS	WAIT	BUSY	ARM	MEMB	MEMA	HFCRE	HFCRD	LFCRE	LFCRD	LFCRS	LFCRF	SE	MERR	NOCLK

Table B-98 Receiver Interrupt Event Register Bit Definition

Field/Bit Definition:

NOCLK	No Clock; Slow or missing clock.
MERR	Memory Error;
SE	Start Error;
LFCRF	Low Frequency Clock Recovery too Fast.
LFCRS	Low Frequency Clock Recovery too Slow.
LFCRD	Low Frequency Clock Recovery too Deviation.
LFCRE	Low Frequency Clock Recovery too Error.
HFCRD	High Frequency Clock Recovery No Data.
HFCRE	High Frequency Clock Recovery Error.
MEMA	Bank A memory busy.
MEMB	Bank B memory busy.
ARM	Receiver armed.
BUSY	Receiver busy
WAIT	Receiver Waiting
TDIS	Trigger Disabled.
TACK	TxAck Signal

Notes:

1. 1 = event true, 0 = event false.

4.1.10 Receiver Revision (RREV:78000_h)

The revision register contains the Data Formatter revision/status code.
Table B-100 lists the bit description of the data formatter/status register.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MODEL																VER								REV							

Table B-100 Data Formatter/Status Bit Definition

Field/Bit Definition:

REV	Revision code.
VER	Version code.
MODEL	Model code.

Notes:

None.

4.2 Receiver Record Memory (RECORD:200000_h)

The bank memory stores the data from the receiver board as well as sync and time stamp data.
The bank memory is stored in an array of 512K by 24 bits illustrated below.

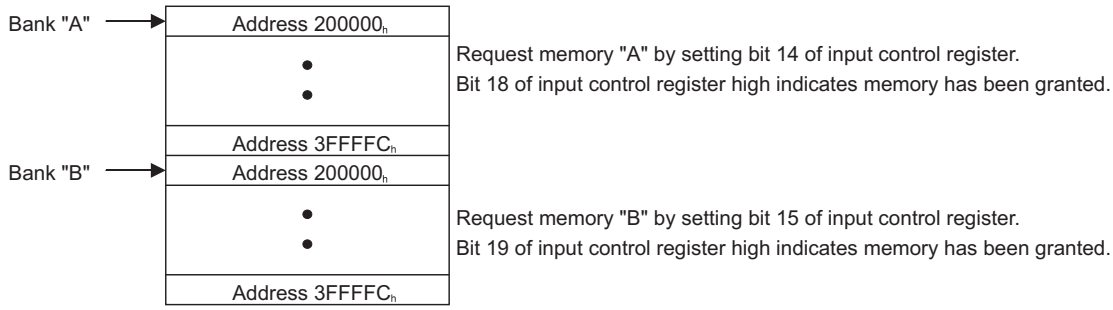


Figure B-16 Receiver Bank Memory Addressing

Table B-101 lists the bit definition of the receiver bank memory.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X								SYNC								GOOD1								GOOD0							

Table B-101 Receiver Bank Memory Bit Definition

Field/Bit Definition:

GOOD0	Good zero memory. (1 = valid low level)
GOOD1	Good one memory. (1 = valid high level)
SYNC	Receiver sync memory. (See description below)

Data is loaded into the GOOD0 and GOOD1 memory from MSB to LSB, i.e., MSB is oldest data bit..

The SYNC byte is used to reconstruct the receiver memory. The following table describes the data fields of the sync byte.

Bit #							
23	22	21	20	19	18	17	16
TYPE DATA					TYPE		

Table B-103 Sync Byte Bit Definition

The “TYPE DATA” field of the sync byte contains data dependant on the “TYPE” field. The following table describes the sync types as well as the sync type data.

Bit #							
23	22	21	20	19	18	17	16
NU					PRE (0)		
TNUM				NU	TRIG (3)		
TSDATA				NU	TS (5)		
NU					POST (6)		
STEP				FULL	TBIT (7)		

Table B-102 Sync Byte Type Description

Field/Bit Definition:

PRE	Preamble or invalid data (invalid data is GOOD0 = GOOD1 = 1, all other combinations of GOOD0 and GOOD1 is pre trigger)
TRIG	Trigger Type (data is post trigger)
TNUM	Trigger number that initiated record sequence.
TS	Time Stamp Type (data is post trigger)
TSDATA	Time stamp nibble (LSN to MSN)
POST	Postamble data
TBIT	Trigger bit flag (data from previous address contains LSB of trigger, data at this address is post trigger)
FULL	Allocated preamble memory full (1 = full)
STEP	Sequence step that initiated the record sequence

Notes:

1. The sync byte at the address prior to the “TBIT” will contain a “1” that indicates the LSB position of the trigger.
2. It takes eight TS types to capture the entire 32 bits of time stamp data.